Compact 4-Bit Carry Look-Ahead Adder in Multiple Output ECDL Gate

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ABSTRACT

A compact 4-bit carry look-ahead (CLA) adder implemented in a single multiple-output enable/disable CMOS differential logic (MOECDL) gate is presented in this paper. The MOECDL proposed here seems to be a very promising multiple-output structure since it takes the advantages of the low dependency to the number of transistors in series provided by the ECDL topology. The 4-bit adder has been designed to demonstrate the functionality and the features of such new logic structure. Electrical simulations have been carried out to validate it taking into account the parameters from a typical 0.35um CMOS process.

1. INTRODUCTION

The differential and dynamic CMOS logic families offer several advantages with respect to standard CMOS logic circuits. The logic function complexity is easily increased in a single gate, providing the output signal and the complementary one. These dual-rail topologies work in two phases or states, being the disable state (output pre-charging phase) and the enable state (logic evaluation phase). The Enable/disable CMOS Differential Logic (ECDL) [2], in particular, is a very promising approach because a single ECDL gate can handle more levels (transistors in series) in a logic tree than the most popular DCVS [1] structure.

Multiple output logic gates, on the other hand, have been proposed for recurrent logic such as circuits based on the carry look-ahead (CLA) adder principle. In this logic style, single logic gates produce multiple functions, and the device count reduction of a factor of 2 or more can be achieved depending on the degree of recurrence in the circuit. A single gate full 4-bit CLA adder has been designed to verify these features.

2. MULTIPLE OUTPUT ECDL GATE

The ECDL structure was originally proposed by Lu [2]. Basically, an ECDL gate has three major components. First, there are two inverters in a latch structure. These are connected to a dual-rail NMOS logic network tree. And then, there are two set transistors that impose a certain logic level to both outputs during the disabled state. In the evaluation phase, depending on the input signals, one output will have a path to ground through the network tree causing an imbalance of voltages between the output nodes, thus setting the latch to the right logic value.

Since the latch discharges the output node, the ECDL structure has no theoretical limitation of number of series transistors in the logic network.

This feature candidates such structure as a very promising alternative for multiple-output logic approach, in which both direct and complementary outputs are provided for two or more functions. A predischarge (or precharge) block, composed of the output latch structure and the reset transistors, is connected to at each output pair. The MOECDL structure proposed here is similar to the MODCVS one [3].

However, in practice, when the number of transistors in series is too large (more than 10), the voltage difference created is not large enough to guarantee the latch transition to the right side. It leads to a random decision and, consequently, a wrong result.

Special attention must be done in the multiple-output networks to avoid the sneak paths due to the bi-directional characteristic of MOS transistor [6].

3. MOECDL 4-BIT CLA ADDER

The multiple-output logic structures are very suitable for logic expressions with recursive output property such as the carry look-ahead (CLA) adder algorithm.

In the CLA adder, making $C(i\text{-}1)$ the input carry for state i, and $A(i)$ and $B(i)$ the ith bits of the input data, then the output carry $C(i)$ can be expressed as:

$$C(i) = G(i) + P(i) \,.\, C(i\text{-}1)$$

where

$$G(i) = A(i) \,.\, B(i) \quad \text{and} \quad P(i) = A(i) \oplus B(i)$$

being $G(i)$ the 'generate' signal, and P(i) the 'propagate' signal.

Expanding this yields:

$$C(i) = G(i) + P(i).G(i\text{-}1) + P(i).P(i\text{-}1).G(i\text{-}2) + \ldots$$
$$\ldots + P(i).G(i\text{-}1) + P(i).P(i\text{-}1)\ldots P(1).C(0)$$

The sum signals are given by:

$$S(i) = A(i) \oplus B(i) \oplus C(i\text{-}1) \quad \text{or} \quad S(i) = P(i) \oplus C(i\text{-}1)$$

The MOECDL 4-bit CLA adder implemented in a single gate is proposed, as illustrated in Fig. 1. The generate and propagate signals are defined into the single network, as well as the XOR functions for the adder outputs $S(i)$. Note that, the propagate signals could also be obtained by using an OR function without logic error in the output carry expression. However, the redundancy of $G(i)$ and $P(i)$ functions for the condition $A(i) = B(i) = 1$ could provide the undesirable sneak paths, discussed before. In this case, transistors with complementary inputs must be added to avoid that trouble, as mentioned in [5].

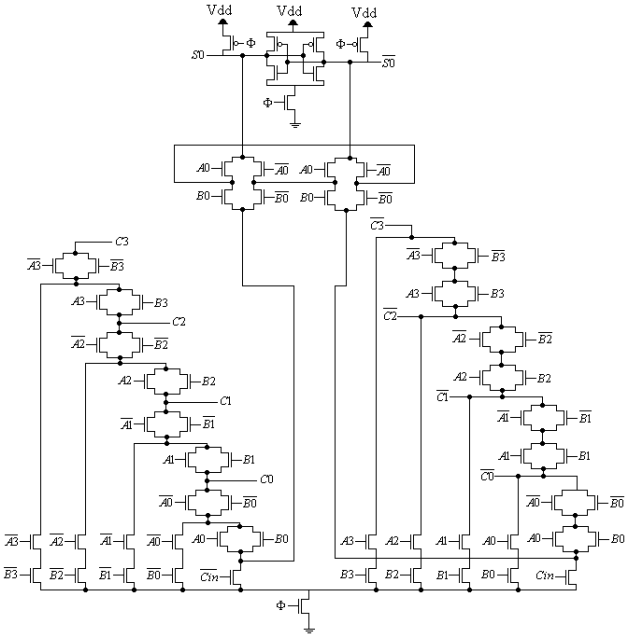

Figure 1. MOECDL 4-bit CLA adder gate.

The correct functionality of the MOECDL 4-bit CLA adder was verified through electrical simulations considering the AMS 0.35um CMOS process parameters. Simulated input vectors are presented in Table I, and the output results S(3)-S(0) and the output carry can be verified in Fig. 2.

Table I. Input vectors used in electrical simulations.

A(3..0)	B(3..0)	S(3..0)	Cout
0001	1111	0000	1
1011	1100	0111	1
0100	0111	1011	0
1110	0000	1110	0
0001	1011	1100	0
1011	1000	0011	1

The proposed adder has been compared to a conventional NAND/NOR CMOS implementations and the MODCVS structure [3], implemented targeting the same fabrication process. The results are shown in Table II.

Table II. Comparison of 4-bit CLA adders.

	Sum delay (ns)	Cout delay (ns)	Power (mW)	# Trans.
NAND/NOR	1.73	1.37	0.99	220
MODCVS	1.40	1.24	1.74	171
MOECDL	1.29	1.02	1.34	138

4. CONCLUSIONS

The novel MOECDL structure was proposed in this paper. A single-gate 4-bit CLA adder has been designed in order to demonstrate the features and potentialities of this promising logic family. The comparison to conventional CMOS and MODCVS logic implementations was realized through electrical simulations, taking into account the process parameters from a typical 0.35um CMOS technology. The results confirmed the performance expectations.

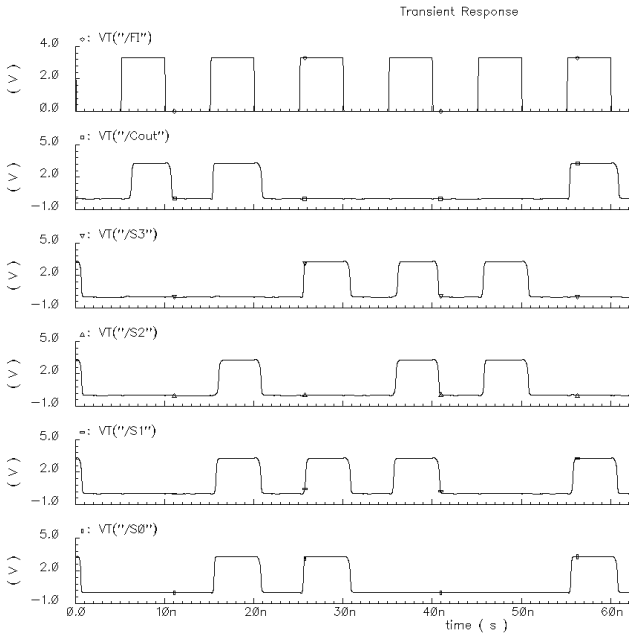

Figure 2. Simulation of MOECDL 4-bit CLA adder gate.

5. ACKNOLEDGMENTS

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