ANALYSIS AND VALIDATION OF AN ANALOG COMPARATOR USING *CADENCE®* ENVIRONMENT

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ABSTRACT

The design of an analog circuit depends on several factors such as good device modeling and technology characterization. In this context, design tools for the circuit implementation and electrical simulations (schematic and layout implementations) are very important to obtain a reliable design. This paper presents some considerations of design, validation and implementation of analog integrated circuits, taking as example the Track-And-Latch Comparator analog block. Some comments about the tool that was used, the Cadence Design Environment, are also presented.

1. INTRODUCTION

The development of VLSI (*Very Large Scale Integration*) technology has resulted in tremendous potential for designing analog circuits. Several VLSI systems require analog sub-systems such as amplifiers, comparators, filters, digital-analog and analog-digital converters, and so on.

This work focuses on the analysis and design of a basic analog circuit block: the Track-and-Latch Comparator. Initially the circuit was analyzed and designed with the parameters and methodology presented in [5]. Then, the circuit was implemented and validated using the CADENCE environment.

2. ANALOG CIRCUIT DESIGN

The objective of analog circuit design is to map signal conditioning constraints into electronic circuit blocks that meet those specifications [1]. This is a challenging task because the analog design procedure is based on several variables, mathematical equations and circuits representations.

The designer must understand the process deeply enough to be able to model, layout, and test his chips. Therefore, the design of an analog circuit depends on several factors such as a reliable design methodology, good modeling and technology characterization.

3. CADENCE DESIGN SYSTEM

Cadence® Analog Design Environment (formerly Analog Artist) is the most complete front-to-back analog design automation solution for full-custom analog and RF IC design. Cadence has integrated a wide range of powerful and proven tools into a comprehensive design flow.

4. ANALOG BLOCK IMPLEMENTATION: THE TRACK-AND-LATCH COMPARATOR

The comparator is a building block for analog integrated circuit design, extensively used in analog-digital (A/D) and digital-analog (D/A) converters. The Track-And-Latch Comparator [2], shown in figures 1 and 2, has NMOS input differential pair M1-M2, inverters M3-M8 and M4-M9 in positive feedback configuration, pre-charge transistors M6-M7, and a current source controlled by the signal phi1 (M5). It has the advantage of low stand-by dissipation, since it shuts down current consumption after the clocked comparison.

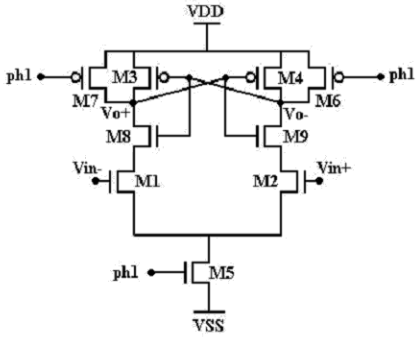

Figure 1 – Track-and-Latch comparator schematic.

The input signals have to de stable during the comparison semi-cycle phi1 (clock). At the rising edge of the clock phi1, the pre-charge transistor are "open" and the differential pair is activated, initiating the comparison. In the pre-charge phase (inactive semi-cycle), the current of M5 (Itail) is turned off and the input drivers are reset and pre-charged Vo+ and Vo- to VDD. The speed of this type of comparator is strongly dependent on the Itail current, that is, speed is directly proportional to the current in M5.

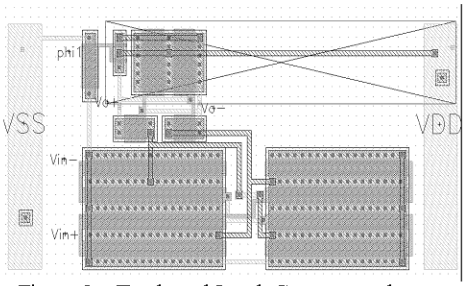

Figure 2 – Track-and-Latch Comparator layout.

The Comparator was designed to meet the following specifications [3] [4]: 5mV sensitivity, 5MHz operating

frequency, C_L = 100fF, SR_{min} = 100V/μs, V_{DD} = 1.65V and V_{SS} = -1.65V.

In order to maintain the output comparator signal stable during the inactive semi-cycle a Latch-D stage is used. The circuit of Latch-D, showed in Figures 3 and 4, is a simple digital circuit composed of two NOR2 gates, two NOR3 gates and two output buffers.

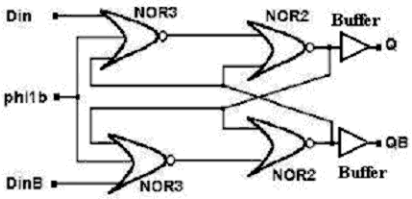

Figure 3 – Latch-D Comparator schematic

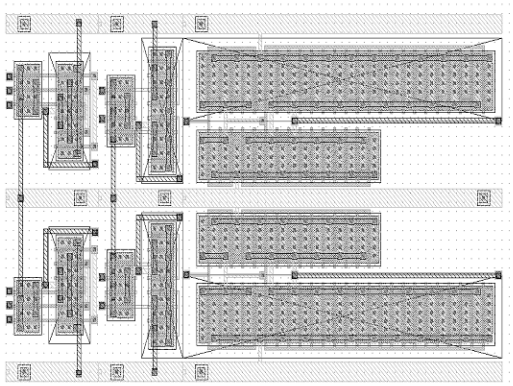

Figure 4 –Latch-D Comparator layout.

The Track-And-Latch Comparator was implemented in 0.35μm CMOS technology, using the CADENCE tool, with a total area of 78 x 50 μm^2 . In figure 5 the complete layout of the comparator can be seen.

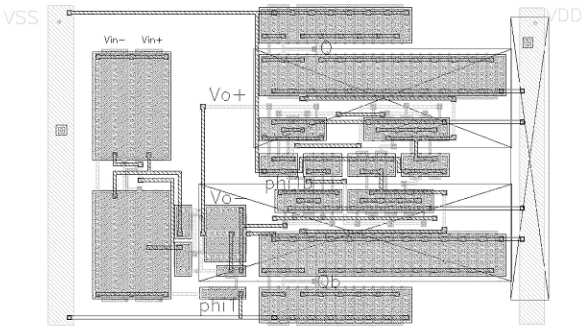

Figure 5 – Complete layout of the Track-and-Latch.Comparator

The simulated (Spectre) performance results are shown in table 1. We can note that the comparator maximum frequency is strongly dependent on the current that feeds the differential pair (Itail).

Table 1 – Simulated comparator performance in 0.35 μm CMOS technology

	Electrical simulation (SPECTRE)	
	Schematics	Post-layout
Delay td_{hl} (ns) $_{phi1 \rightarrow Vo+}$	8.63	7.88
Delay td_{lh} (ns)$_{phi1 \rightarrow Vo+}$	5.15	5.20
$f_{máx}$ (MHz)	70	69
Sensibility ΔVin(Vp) @ 10Mhz	0.5m	1m
Itail (μA)	63.5	65

5. CONCLUSIONS

The comparator block pre-defined in [3] was implemented using Cadence Environment. The design methodology was validated with electrical simulations (schematic and post-layout).The re-simulation has provided some additional conclusions referring to analog circuit design and the Framework Cadence Design Environment.

ACKNOWLEDGEMENTS

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7. REFERENCES

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