TEST SCHEDULING AND BENCHMARK IMPLEMENTATIONS FOR THE ANALYSIS OF SOC TESTING

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ABSTRACT

This paper presents two aspects of the test of core-based system-on-chip. The first one refers to the implementation of a test scheduling algorithm for a bus-based test access mechanism. The second one refers to the implementation in VHDL one of the ITC'02 SoC Test Benchmark together with a test access mechanism that is based on the reuse of the hardware already available in the system. Whereas the first work represents a good exercise for the understanding of the complexity of the system test, the second one will probably be extensively used to validate of techniques developed in this research group.

1. INTRODUCTION

The current requirements for good performance, low cost and reliability of electronic circuits created a new paradigm in the design of integrated circuits. The diverse functionalities of a system moved to the inside of a single chip, forming a SoC (System-on-Chip). The development of a complex system was changed to an integration of several modules (cores) under a logic defined by the system designer. These independent modules can be bought from different manufacturers and in different forms of description, as well as used in systems of distinct functionalities.

This change generated new requirements for the project, mainly during the system integration. In this phase, the system integrator (designer) must provide conditions for the verification of the correct system operation, what consists in the adequate functioning of each module that defines the system logic. To perform such verification, it is necessary the test of each core embedded into the system, and the provision of the requirements that the test of each core demands. The test planning and the transport mechanism of the test data to each core also must be provided by the designer.

The test of those complex systems is still an important research subject and diverse solutions have been presented in the last years. These solutions work with four basic parameters for the test of the SoC: test time, area overhead for components added to the logic, number of extra pins in the system interface, and power consumed during the test. The performance of the test is a trade-off among those parameters and it is not possible to establish an optimum solution, since the importance of each parameter for the cost of the system can change from one project to another. In this paper, two possible test solutions for a SoC are discussed. The first one is a bus based test scheduling algorithm implementation. The second one is a benchmark system implementation in VHDL.

The paper is organized as follows: Section 2 reviews some test concepts algorithms and its costs. Section 3 presents a test algorithm implementation with its results analysis. Section 4 refers to a SoC test benchmark implementation in VHDL. Section 5 concludes the paper.

2. TEST PLANNING FOR CORE-BASED SYSTEMS-ON-CHIP

The test of a SoC can be divided into different levels. For the complete test of the system, the verification of the cores and the internal connections are necessary. For the test of the cores it is necessary the transport of the test vectors from the system interface to the cores under test as well as the transport of the test responses of the core back to the system interface. Additionally to this process, the test scheduling, that determines the moment where each core is tested, is an important issue.

The transport of the test data inside the chip is one of the main aspects that differ the algorithms. In general, there are two types of solutions: reuse of functional connections and creation of buses exclusively for the test. The choice of one of these forms of transport has direct consequences on the test costs usually the reuse based solution presents a lower area overhead and lower number of test pins than the solution of dedicated test buses on the other hand, this last one presents a smaller complexity for the planning and scheduling of the test, since all cores can be directly accessed from the system interface, without using other cores for the transport of the test vectors.

The commercial SoC's are usually protected by intellectual property laws. Therefore, VHDL descriptions of industrial systems are not available. To have a SoC description for doing tools tests, Marinissen *et al* [5] proposed a set of SoC test benchmarks whose main goal is "to stimulate research into new methods and tools for modular testing of SoCs and to enable the objective comparison of such methods and tools with respect to effectiveness and efficiency.' ' The benchmarks provide the cores test requirements in terms of number and type of tests, number of test patterns, and cores test interface

(number and size of internal scan chains, number of test pins, hierarchy level of the core).

3. TEST SCHEDULING FOR A BUS-BASED TEST ACCESS MECHANISMS

Considering a bus-based TAM, the Iterative Rescheduling [2] algorithm was implemented to define the system test scheduling. The algorithm was validated for the d695 ITC'02 benchmark, an academic example of an SOC composed by ten modules from the ISCAS'85 and ISCAS'89 sets. The principle of functioning of this algorithm is simple. It chooses one core and moves this core from its slot time to another slot time. This process is done to every core in the system and to every slot time in the scheduling. If the resulting scheduling, the scheduling after a move, has a smaller cost than the original scheduling, this new scheduling is saved and become the original scheduling to next iteration. To the correct functioning of this algorithm, there are two requisites: 1) it must be assumed that each core can be accessed from the system interface, what consists in a bus-based test solution. 2) there is an initial scheduling where the changes will be done. For the analysis, the initial scheduling was generated by [1]. As this tool assumes system connections reuse, the initial scheduling must be adapted to this solution.

4. BENCHMARK IMPLEMENTATION FOR REUSE-BASED TEST ACCESS MECHANISM

In [1] a test planning tool is proposed. This tool proposes a comprehensive test planning model for the system. The model privileges the reuse of system resources aiming at the optimization of a number of cost factors. The main contributions of this model are threefold: 1) it does not assume a single type of connection for the internal TAMs in the system. Partial test buses are considered, along with functional connections, transparency, and other bypass modes available through the wrapper or the core configuration; 2) the solution does not fully optimize every single core in the system. Instead, the diversity of test requirements among the cores is exploited, by privileging critical cores with more test resources; 3) both the schedule and the global TAM are defined together, and not as independent tasks as in other approaches. This aspect allows the exploration of the design space, so that good compromises among the various trade-offs being sought in the system synthesis can be found.

In order to validate the results of the test planning tool, the system d695 is being implemented in VHDL. This system is a hypothetical system described in the ITC'02 Test SoC Benchmarks set that is constituted by ten cores described in VHDL. This implementation will make possible the analysis of test aspects, such as area and number of estimated clock cycles for testing. In addition to the cores, test auxiliary structures had been characterized, the wrappers. These structures present memory cells that facilitate the cores test. They have some required logic, defined by the IEEE P1500 standard [3]. To implement these wrappers in VHDL a basic model previously developed in this research group [4] was enhanced. The area overhead provoked by the use of these auxiliary structures is being evaluated.

5. CONCLUSIONS

This article presented a revision about test of SoCs, being distinguished its parameters and its algorithms. Additionally, the behavior of these parameters could be observed with the presentation of the results acquired with the implementation of a test scheduling for dedicated test buses. With the objective to supply a contribution to the integrated systems test, the implementation of a benchmark system in VHDL was also presented.

This implementation expects to improve the analysis of test tools performance through the verification of the results calculated with the synthesis of the circuit under test to a technology, making possible the analysis of some parameters of test, like area, with more precision.

With this implementation, it is desired to carry through quantitative measured for the validation of the tool proposed in [1]. This implementation can be further used to evaluate and validate bus-based solutions as well. In addition, the implementation of a NOC (Network-on-Chip) for functional connection of the embedded cores will be implemented, and the reuse of this structure for test will also be validated. Another future work is the implementation of an aid tool that automatically generates P1500 wrappers in VHDL considering a previously defined TAM.

6. REFERENCES

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