A 0-10dBm, 915-927.5 MHz, 0.35 ìm CMOS CLASS E POWER AMPLIFIER WITH DIGITAL POWER CONTROL AND DIRECT MODULATION

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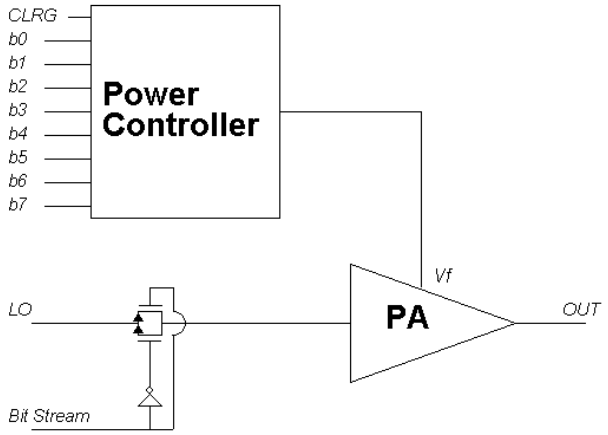
ABSTRACT

This paper presents a 0-10dBm, 915-927.5 MHz, 035ìm CMOS class E power amplifier. This amplifier is part of a SoC under development in our laboratory. Patterned ground shields are used to enhance the inductors' quality factors. The amplifier efficiency is about 45-48%. The input signal of the power amplifier is OOK directly modulated and its output power is controlled by a PWM with digital controller.

1. INTRODUCTION

A System on Chip is being developed [1] for an autonomous, wireless, Irrigation Control System , which requires low power and high efficiency design. The specifications for the PA design presented are OOK modulation, maximum 3.3V bias voltage, 50Ù output impedance and 915-927.5 MHz band operation. As the modulation specified above is non-linear, a non-linear power amplifier configuration may be chosen. Non-linear power amplifiers present higher efficiency than linear ones. Class E and class F power amplifiers are the most popular non-linear configurations. Class E was chosen due to its lower power consumption and reduced number of resonant elements, which results on smaller chip dimensions [2].

The block diagram of the power amplifier with digital power control and OOK direct modulation is shown in Fig. 1.



direct modulation

The block PA in Fig. 1 represents the drivers and the class E power amplifier. The signal from the frequency synthesizer (LO) is directly modulated by the gate transmission, which is controlled by the information signal (Bit Stream).

The output power of the PA is controlled by a PWM, which varies the feeding voltage, V_f, of the class E power amplifier. The PWM pulse width is digitally generated. The power controller receives 8 bits, b0-b7, that determines the pulse width of the PWM signal control. The bit CLRG is an enable bit, which determines whether the power amplifier must operate.

2. POWER AMPLIFIER

2.1. Class E Power Amplifier Configuration

The class E power amplifier was proposed by Nathan O. Sokal and Alan D. Sokal [3] in 1975. The topology used in our design presented in Fig.1 [2,4], which is a modified version from the classical topology [2,3].

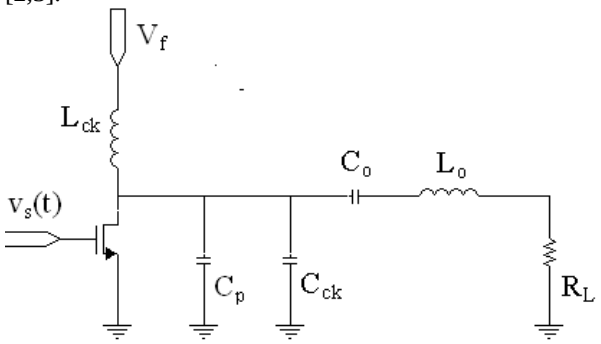


Fig. 2 – Class E Power Amplifier Topology

In the circuit presented in Fig.2, the transistor is considered a perfect switch. For maximum efficiency the input signal, $v_s(t)$, must be a pulse waveform with duty cicle of 50% [3-5]. The series resonant circuit formed by Lo and Co is an output band-pass filter tuned to resonate at the first harmonic of $v_s(t)$ [3,4]. The capacitance C_p ensures no drain-source dissipation in the on-off transition of the transistor [2]. In fact, C_p creates a delay between drain voltage and current during the on-off transition.

L_{ck} and C_{ck} resonates at the second harmonic of $v_s(t)$, which implies that the class E amplifier operates similarly at the class F amplifier [2]. In the classical topology, L_{ck} is an ideal RF chock, what is not true in

the real case. The addition of C_{ck}, proposed by [4] permits a more realistic design.

2.2. Power Amplifier Design

The power amplifier was designed combining the analysis presented in [4] and [5]. The first one considers the influence of finite dc-feed inductance, i.e, L_{ck} as a non-ideal RF chock. As mentioned earlier, C_{ck} is included to resonate at the second harmonic of $v_s(t)$. The second one considers the influence of the finite output band-pass filter´s quality factor formed by L_o and C_o.

In the design, primary is considered the influence of the finite output band-pass filter's quality factor, which influences strongly on the harmonics of the output under R_L. The circuit obtained from this first analysis is then used to determine the final power amplifier circuit elements shown in Fig. 2 [2].

The most critical elements in the power amplifier design are the inductors, which equivalent circuit when using patterned ground shield can be determined following the analysis presented in [2,6]. If the process parameters are known, each element of the equivalent circuit can be evaluated. The ohmic losses of the inductors can be more precisely evaluated if the current crowding effect is considered [6,7].

The power amplifier was designed for AMS, 0.35ìm CMOS, 4 metal and 2 poly process. The values for the elements given in Fig. 2, after the inclusion of all parasitic elements, are given in Table 1. The values of feeding voltage for 0dBm and 10dBm output power are, respectively, 0.3V and 1.0V, with efficiency about 45-48%.

R_L	L_o	C_o	L_{ck}	$L_{ck}+C_{ck}$	W/L
50 Ù	7.74nH	3.85pF	5nH	1.4pF	1250

Table 1 – Element values for the class E power amplifier

The value for $L_{ck}+C_{ck}$ considers that part of them are included in the drain-source capacitance of the transistor and the parasitic capacitances C_{ox}'s of the inductors.

The output voltage under R_L for 10dBm is shown in Fig. 3 .As can be seen, the second harmonic of the output power is about 15dB below the first harmonic.

By using 8 bits for power control, as shown in Fig. 1, and considering the PWM operating at 1.2V, it is possible to achieve 0.2dB output power variation.

3. CONCLUSION

A low voltage class E power amplifier with power control and OOK direct modulation is proposed. The design of the class E power amplifier was presented, although the another circuit blocks shown in Fig. 1 are designed for AMS, 0.35ìm CMOS, 4 metal and 2 poly process.

The power amplifier can deliver 11.5dBm to the load with 1.2V feeding voltage. For 0-10dBm the power amplifier efficiency is about 45-48%.

4. REFERENCES

[1] http://www.ccs.unicamp.br/scmn

[2] L. S. Assunção, *Relatório de Atividades de Bolsa mestrado* , Processo PROCAD nº0172/00-6, Departamento de Engenharia Elétrica da Universidade de Brasília-ENE/FT/UnB, Maio 2003.

[3] Nathan O. Sokal, Alan D. Sokal, "Class E – A New Class of High Efficiency Tuned Single Ended Switching Power Amplifiers," *IEEE Journal of Solid State Circuits*, Vol 10, Nº03, pp 168-176, June 1975.

[4] C. K. T. Chan, and C. Tomazou, "Design of a Class E Power Amplifier with Non-Linear Output Capacitance and Finite DC-Feed Inductance," *IEEE International Symposium on Circuits and Systems*, Vol 1, pp 1129-1132, 2001.

[5] M. K. Kazimierczuk, and K. Puczko, "Exact Analysis of Class E Tuned Power Amplifier at any Q and Switch Duty Cicle," *IEEE Transctions on Circuits and Systems*, Vol CAS-34, Nº02, pp 149-159, February 1987.

[6] S. S. Mohan, C. Yue, M. del Mar Hershenson, and T. H. Lee, "Modeling and Characterization of On-Chip *Technical Digest on IEEE International Electron Devices Meeting*, pp 531-534, 1998.

[7] W. B. Khun, and N. Ibrahim, "Analysis of Current Crowding Effects in Multiturn Spiral Inductors," *IEEE Transactions on Microwave Theory and Techniques*, Vol 49 Nº01, pp 31-38, January 2001.

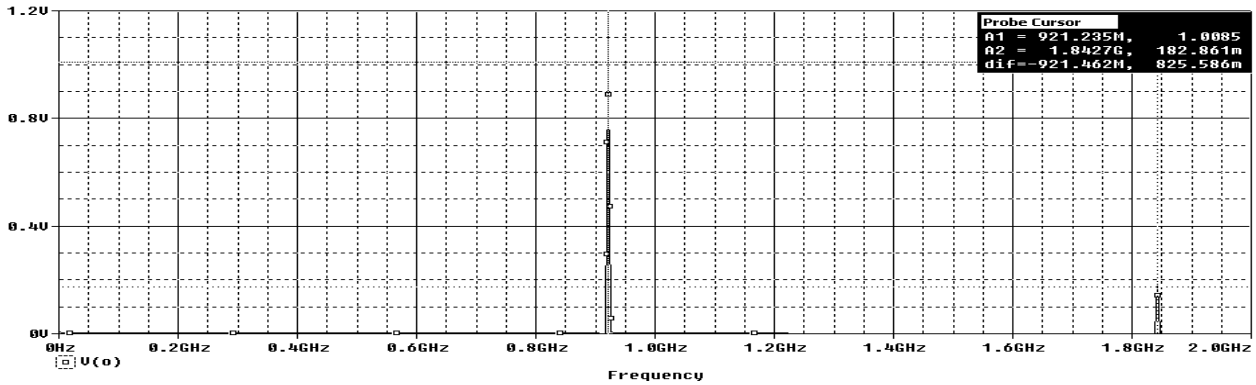


Fig. 3 – Output voltage for 10dBm output power