XINGÓ: A PROTOTYPING PLATFORM WITH PROCESSING CAPABILITIES

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ABSTRACT

In this work we present a hardware platform to support the design, testing and verification of embedded systems that require prototyping. By analyzing the characteristics and necessities of those projects we could summarize an unique and generic platform, which is based on the Algorithmics P-4032 prototyping kit, but not exclusively dependent on it to work. The platform has made possible the implementation of new hardware that is always common on reconfigurable computing. On the other hand, the onboard MIPS processor brings much more power and flexibility to the whole platform. At the end of this work we obtained such platform, which could satisfy all the original necessities, capable of working alone, with no connections to the kit, and also having the FPGA working either as a processor or as a co-processing unit.

1. INTRODUCTION

The advance in the computer-aided design area has favored the design of embedded systems with low cost and high performance. On this methodology, the entire system is developed using several third part cores, which were appropriately tested and validated. The designer task is to choose among the available cores, the ones that will be used on his project. However these brand new systems have sometimes, not only to be simulated but also tested and validated before they reach the market. One of the many ways of achieving that goal is to use prototyping platforms.

Some projects of the Computer Systems Laboratory (LSC), at Institute of Computing, have involved reconfigurable computing as well as code compression for embedded systems. Many of these have the goal of prototyping, but at that time there was not a suitable platform. The unique available platform was an Algorithmics P-4032[1] prototyping kit, using a MIPS processor, without possibilities of implementing new hardware. These problems motivated the implementation of an additional board that could be used with the P-4032 kit, and thus complement it with prototyping capabilities.

On the section 2 we present some prototyping platforms and the reasons that they were not used. The section 3, describes the project and implementation steps, while on the section 4, the obtained results are shown, as well as the possible use cases.

2. RELATED WORK

Nowadays, with the growth of the reconfigurable computing, some prototyping platforms have become available. As an example we could cite the XESS XSV800 Development Kit, which contains a lot of hardware interfaces tied to a 800k gates FPGA. Other manufactures have their similar boards like Avnet, Pender Electronics but none of them have a real support for intercepting the CPU signals before the system bus as required in the code compression hardware[3,4].

Though, those platforms cannot be connected with the P-4032 kit, and do not have any processing capabilities, so obviously becoming inappropriate for use on the LSC projects.

3. DEVELOPMENT

The development of this prototyping platform was strongly based on the analysis of the P-4032 kit and the R4000 processor. This processor comes in daughter board, and the key idea is to remove it, and insert the Xingó platform in its place.

The first part of the project was to design the board architecture and also determine the component interconnections. Considering that the board should also support a memory bank and the configuration circuitry, as well as its small size, we could note very early how hard the circuit board routing was going to be. So we spent great attention on the schematic project, in order to simplify the routing.

However the available routing tools could not take advantages of those facilities, resulting in an unsatisfactory board routing, driving us to manual routing, using a four-layered printed circuit board (PCB), which is shown in Figure 1. It was a really hard task trying to optimize the track paths and at the same time minimize the interconnections. In order to prevent signal noises, two layers for the power supply planes were used.

In a second moment, we have the PCB manufactured, soldered the components, and finally we have done some functional tests, resulting in a platform ready for use, which can be seen in the Figure 2.

4. RESULTS

The main goal of this project was not only to provide a good prototyping platform, but also, one that could be used in future projects. Besides the MIPS R4000 processor, there are on the same board a memory bank, both connected to the FPGA.

The APEX FPGA (EP20K200) [2] can be configured using the JTAG and also the Bit Blaster connectors. A configuration circuit, based on two EPC2 chips, was also included providing the automatic configuration and a certain computer independence.

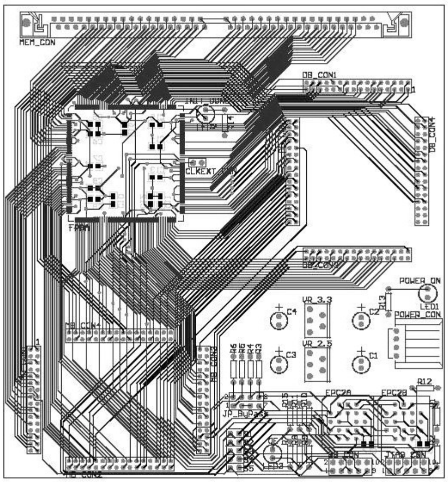

Figure 1: Xingó's PCB routing

Thus the project resulted in a platform with three main uses, which are described below.

4.1. The Stand Alone Use

The first possible use of the platform takes advantage of its independence of the P-4032 kit. There is an build-in power supply and an external clock connector that allows the implementation of a great variety of hardware on the FPGA, having on their disposition a processor and a memory bank. This configuration can be successfully used on research in companies as well as at universities.

4.2. The FPGA as Processor

We can get in trouble if we try to experiment a different kind of processor on the P-4032 kit, because there is no adequate socket for it. The new processor signals might be quite different of that expected by that kit. Since we have in hands a VHDL, Verilog or SystemC synthesized description of a processor, we can try it on the platform, just by configuring the FPGA. Of course we should adequate the signals, but this is not an impossible task as before. The memory bank and the R4000 processor can also be used by the new-implemented processor. We could cite the case of testing a new instruction set, when the designer could collect data of real tests running in such FPGA, making easier the verification of those new instructions. This can be quite useful for reconfigurable computing projects.

4.3. The FPGA As Extra Processing Unit

The last case shows the use of the R4000 processor with a FPGA placed between it and the P-4032 bus. This is extremely interesting when we want to implement a kind of coprocessor on the FPGA. One of the main motivation of developing this new platform, was to allow the implementation of an execution time code decompressor. Such project should communicate to the R4000 processor and the main board at the same time it accesses the memory bank. The memory would contain the compressed executable code, which was going to be decompressed on the FPGA, and then sent to the R4000 processor to be executed.

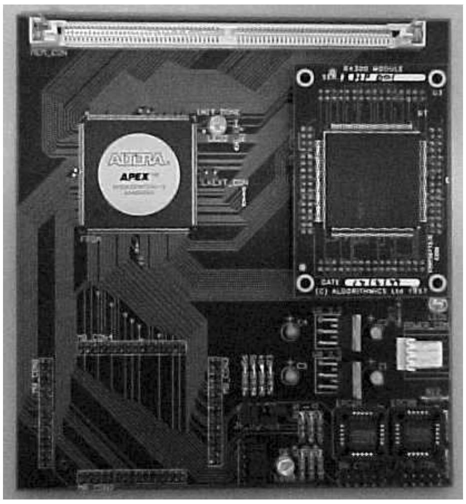

Figure 2: The Xingó's PCB

5. CONCLUSIONS

In this paper we have presented the developed prototyping platform based on the Algorithmics P-4032 kit. The necessity of implementation of such board arose during the developments of some projects involving embedded systems at the LSC, and because of the nonexistence of a better platform for testing and prototyping them.

Its main feature is the ability of being sufficiently generic and flexible, and due to this, capable of supporting a wide variety of applications.

6. REFERENCES

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[4] Guido Araujo, Paulo Centoducatte, Rodolfo Azevedo and Ricardo Pannain, "Expression Tree Based Algorithms for Code Compression on Embedded RISC Architectures", *In IEEE. Trans. on VLSI Systems*, October 2000.