

Study of Device Parameter Extraction in SOI nMOSFETs

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Abstract – This article presents experimental results obtained for threshold voltage (V_{th}), transconductance (g_m), subthreshold slope (S), series resistance (R_{series}) and effective channel length (L_{eff}) in SOI-MOSFET devices using conventional methods applied in bulk MOSFETs.

I. INTRODUCTION

The SOI-MOSFET device is a transistor with an insulating layer between the channel region and the substrate. Figure 1 illustrates the cross-section of an SOI-MOSFET.

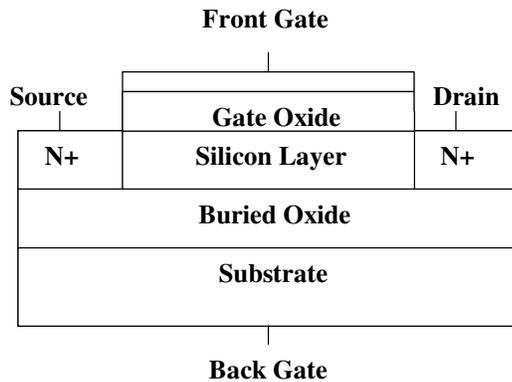


Figure 1: SOI-MOSFET cross-section.

This insulating layer isolates the device active region and the underlying substrate, leading to improved transconductance, reduced short-channel effects and quasi-ideal subthreshold slope [1][2].

The goal of this work is to investigate the MOSFET properties of threshold voltage, subthreshold slope, transconductance and series resistance in SOI transistor using the common techniques applied to bulk MOSFETs.

The devices used in this study are fully depleted SOI MOSFETs with thickness of 30nm for the gate oxide, 80nm for the silicon film and 390nm for the buried oxide. An L-array of devices with 10 μ m, 5 μ m, 3 μ m, 2 μ m, 1,5 μ m and 1 μ m long transistors with channel width of 20 μ m has been used in the experiments.

II. THRESHOLD VOLTAGE

The method used to extract the threshold voltage was the double derivative $I_{DS} \times V_{GS}$ curve, where the maximum positive peak corresponds to the threshold voltage value [3].

The figure 2 shows the typical $d^2I_{DS}/dV_{GS}^2 \times V_{GS}$ curve where is extracted the threshold voltage.

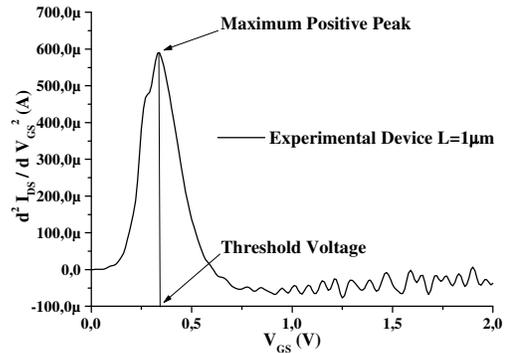


Figure 2: Experimental double derivative $I_{DS} \times V_{GS}$ curve with the maximum positive peak indicating the correspondent threshold voltage value.

There is an excess of noise corresponding at the second derivative curve in the experimental device and, sometimes, it is necessary to use a fast Fourier transformer filtering to reduce it.

The value extracted was 0,34V for a 1 μ m long device.

III. TRANSCONDUCTANCE

It is possible to obtain the transconductance (g_m) using a single differentiate $I_{DS} \times V_{GS}$ curve.

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{W\mu_n C_{ox}}{L} V_{DS} \quad (1)$$

where: W = channel width; μ_n = electrons mobility in inversion layer; C_{ox} = oxide capacitance; L = channel length.

As can be seen in transconductance equation (Equation 1), this parameter is directly proportional to the mobility and consequently it is the respective point for maximum mobility.

The figure 3 shows the point of maximum transconductance in a 1 μ m SOI MOSFET, which extracted value was 127,3 μ A / V.

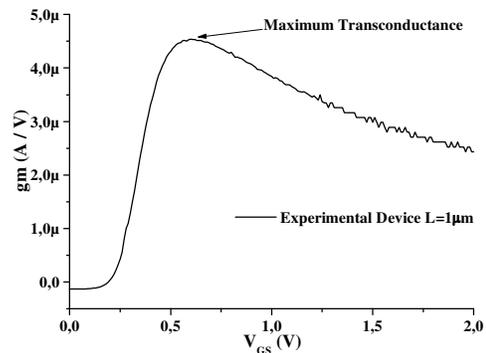


Figure 3: Experimental single differentiate $I_{DS} \times V_{GS}$ curve, with the indication of maximum transconductance point.

Figure 4 shows the maximum transconductance as a function of device channel length for studied technology.

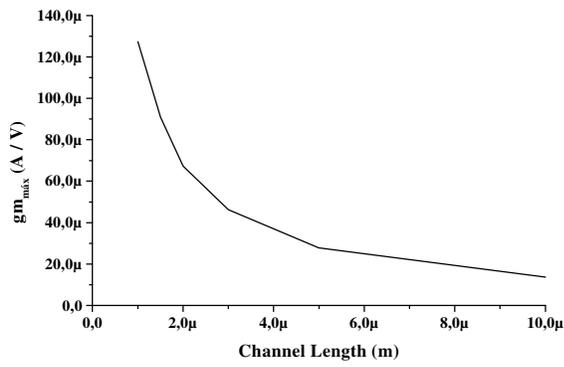


Figure 4: Comparison of maximum transconductance for different length channels to experimental devices.

Figure 5 shows the mobility also as function of device channel length for studied technology.

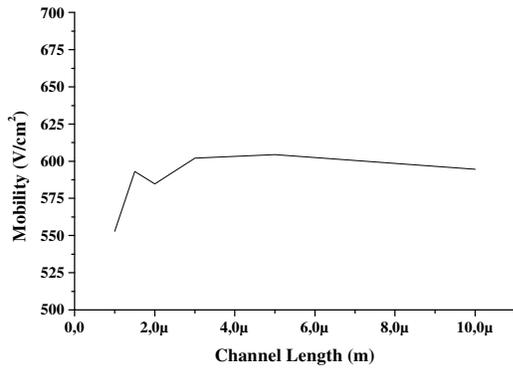


Figure 5: Mobility x Channel Length curve shows diminution in mobility as the channel length reduces.

IV. SUBTHRESHOLD SLOPE

The subthreshold slope is defined as:

$$S = \frac{dV_G}{d(\log I_D)} = \frac{kT}{q} \ln(10) \left(\frac{1 + C_{SID}}{C_{ox}} \right) \quad (2)$$

where: k = Boltzmann constant; T = temperature; C_{SID} = silicon film capacitance.

The figure 5 demonstrates the experimental curve $\log I_{DS} \times V_{GS}$ to extract the subthreshold slope and a comparison of different channel length devices.

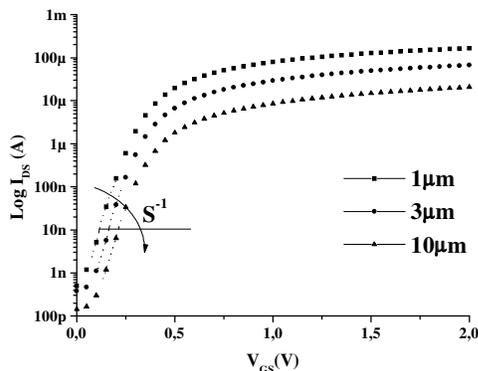


Figure 5: Log $I_{DS} \times V_{GS}$ curve, indicating subthreshold slope for SOI-MOSFET devices with different channel lengths.

The SOI transistors measured had a similar behavior, with subthreshold slope values about 70mV to different channel lengths. These values indicate a fully depleted behavior of the SOI transistors.

V. SERIES RESISTANCE AND EFFECTIVE CHANNEL LENGTH

According to John G. J. Chern method [4] it is possible to extract the series resistance and calculate the effective channel length in a single curve.

In a graph of Total Resistance x Channel Length, with fixed values of V_{GS} (Fig. 6), is obtained curves which will touch in a coincident point known as $R_{series} \times \Delta L$. At this point two values are extracted: the series resistance (R_{series}) and the difference between effective channel length and channel mask length (ΔL).

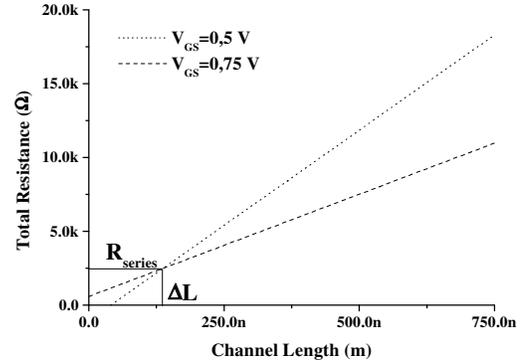


Figure 6: Total Resistance x Channel Length graph with a group of V_{GS} curves to experimental devices; the point of intersection gives the R_{series} and ΔL .

Using the equation 3 we can calculate the effective channel length:

$$L_{eff} = L_{mask} - \Delta L \quad (3)$$

where: L_{eff} = effective channel length; L_{mask} = channel mask length; ΔL = difference between effective channel length and channel mask length.

The SOI-MOSFET devices used to extract the series resistance and effective channel length had 1, 1.5, 2, 3 and 5 μm channel lengths. The approximated extracted values to R_{series} and ΔL , respectively, are: 2.4K Ω and 137nm (experimental).

VI. CONCLUSION

This paper presented experimental results in parameters extraction to SOI-MOSFET devices using parameters extraction methods conventionally used in bulk MOSFETs.

VII. ACKNOWLEDGMENT

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VIII. REFERENCES

- [1] Jean – Pierre Colinge, “Silicon – On – Insulator Technology: Materials to VLSI”, 2nd Edition.
- [2] M. A. Pavanello, “Influência do Substrato no Transistor SOI MOSFET em Temperatura Ambiente (300K) e em Baixa Temperatura (77K)”, M.S. Thesis, Department of Electronics Engineering – LSI – USP, São Paulo, Brazil.
- [3] Terao, A. et al. “Measurement of Threshold Voltages of Thin-Film Accumulation Mode PMOS/SOI Transistors”, IEEE Electron Devices Letter, v.12, n. 12, p.682, 1991.
- [4] A. S. Nicollet, “Estudo da Resistência Série e do Comprimento Efetivo de Canal em Transistores MOS Convencionais e SOI MOS”, M.S. Thesis, Department of Electronics Engineering – LSI – USP, São Paulo, Brazil.