Shallow n^+-p junctions in Si and SIMOX

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ABSTRACT

The reduction of device dimensions allows higher device density on a chip, faster data processing and less power consumption. In this work a study on different processes for shallow n^+-p junctions in Si and SIMOX was done. As or Sb implantation was done to introduce the n-dopant species. The implantation was followed by a conventional furnace or rapid thermal annealing. The electrical (sheet resistance, activation, mobility and charge carriers profile) and physical (dopant and damage profiles) characteristics were measured. The best results were obtained for SIMOX and for the rapid thermal annealing process.

1. INTRODUCTION

The constant miniaturization of microeletronic devices requires that all the device parameters are scaled down simultaneously. For example, in a MOSFET, when the channel length is reduced, it is also necessary to reduce the gate dielectric thickness, the source and drain junctions depth and so on. Typically, the approximate relation between the channel length and the source and drain junctions depth is x_j=0.4L [1], where x_j is the junction depth and L is the channel length. It is important to follow this scaling rule, specially for short channel devices, otherwise many undesired effects, known as short channel effects, like source to drain punchthroug breakdown and high subtreshold leakage current, may appear [2]. In all cases the device operation is strongly affected and is no longer possible to have control over it, in other words, the MOSFET will allow the current passage for a lower value of V_T than it was projected for and there will also be greater power consumption due to higher leakage currents. All these problems can be avoided via fabrication of shallow source and drain junctions for the MOSFETs. The accomplishment of such junctions requires a very short range penetration of the dopant ions into the substrate [3]. The ion implantation is one of the most appropriate techniques for this kind of process. The dopant penetration depth and concentration in the substrate are controlled by choosing the ion implantation energy and dose, respectively. These two parameters can be chosen separately, which is a big advantage of ion implantation over other techniques like thermal diffusion. One of the disadvantages of ion implantation is the need of a thermal annealing step for dopants activation and crystal damage recovering since the implantation destroys the crystal lattice [3].

In the present work the electrical and physical characteristics of As and Sb implanted n^+-p junctions in Si and SIMOX were studied. The goal is to obtain a low resistivity n-type layer over a p-type substrate, low dopant redistribution during the annealing step, low damage concentration, high dopant activation and high carrier mobility. RTA and furnace annealing were performed. The differences between Si and SIMOX results have been discussed.

2. EXPERIMENTAL PROCEDURE

Two different substrates were used in the experiment: Si and SIMOX. The Si substrates were implanted with two different dopant species, As or Sb. The SIMOX substrate was implanted only with As. The implantation energy and dose were 20keV and $5.10^{14}cm^{-2}$, respectively, for both dopants. So there were initially three groups of samples: Si implanted with As, Si implanted with Sb and SIMOX implanted with As. After implantation, the samples were submitted to two different thermal annealing steps. Again, each sample went through only one annealing step. The furnace annealing was done in a conventional industrial furnace at a temperature of 950ºC for 15 min. The rapid thermal annealing (RTA) was done with halogen lamps at a temperature of 1000ºC for 10s with a temperature raise rate of 50ºC/s. At this point there were already six groups of samples: Si(As, RTA), Si(As, furnace), Si(Sb, RTA), Si(Sb, furnace), SIMOX(As, RTA) and SIMOX(As, furnace).

3. ELECTRICAL MEASUREMENTS

Table 1. Electrical results for As implanted Si and SIMOX after RTA and furnace annealing

	Si		SIMOX	
	RTA	Furnace	RTA	Furnace
R_s (ohm/sq)	231	307	225	292
Electrons per cm^2	$4.3x10^{14}$	$2.7x10^{14}$	$4.7x10^{14}$	$2.9x10^{14}$
Activation (%)	86	54	94	58
Mobility (cm^2/V.s)	63	75	59	73

Van der Pauw devices were prepared using photoligraphy. These devices were used for the electrical measurements. The results obtained for the As doped

samples are summarized in table 1. It is seen from these data that the rapid thermal annealing is superior to the furnace one, from the electrical point of view. It is also seen that SIMOX has improved electrical characteristics over Si. The reason for that is not clear yet and is still being investigated.

4. RBS DATA

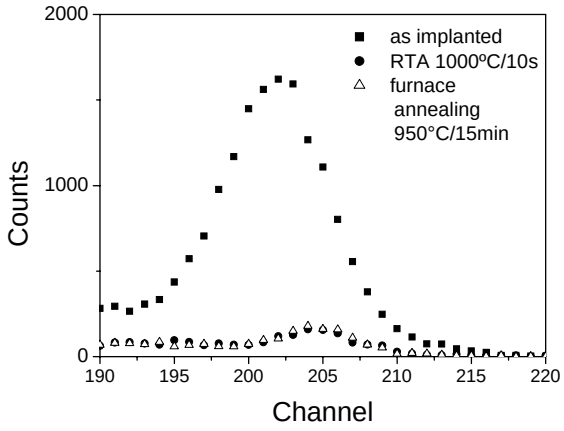

Figure 1. RBS channeling spectra of silicon surface before and after annealing steps. Both annealing processes showed the same efficiency in the removal of implantation damage from silicon crystal lattice.

The dopant profile before and after the annealing steps were obtained via RBS and channeling techniques.

From the spectra shown in figure 1 it is possible to see that the annealed crystal damage was removed after RTA and furnace steps. The spectra for Si and SIMOX were identical in the silicon surface region. It can be seen that both annealing processes efficiently removed the crystal damage caused by implantation. Further analysis revealed that there is no dopant redistribution during RTA in both substrates and also that better As atoms substitutionality in the Si lattice was obtained in the SIMOX substrate. In the case of furnace annealing, some dopant redistribution was observed. There is no significant difference between the profiles of As in Si and SIMOX after furnace annealing. Again, RTA and SIMOX showed better results than furnace annealing and Si, respectively.

5. ANODIC OXIDATION

The charge carrier profiles were obtained via anodic oxidation method [4, 5]. The equipment shown in figure 2 was specially built for this purpose. Only the Si samples were measured. For the SIMOX samples a few changes on the equipment will be necessary due to the insulating layer inside the substrate.

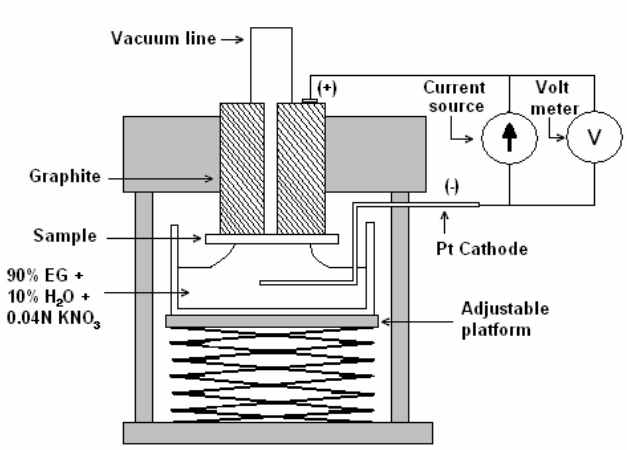

Figure 2. Anodic oxidation equipment used for charge carrier profile measurements.

6. CONCLUSIONS

The rapid thermal process showed to be better than the furnace one both for the electrical and for the physical characteristics of the samples. In the RTA annealed samples we observed less dopant redistribution during the annealing step, higher dopant activation and lower sheet resistance. Comparing both different substrates, SIMOX always had better results than Si. The SIMOX samples showed better implantation damage removal, higher dopant activation and lower sheet resistance. The reasons for SIMOX better performance are not clear yet and need further studies.

7. REFERENCES

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