# IMPLEMENTATION OF A CONTINUOUS MODEL OF ADVANCED SOI MOS TRANSISTORS USING MATLAB

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## ABSTRACT

This work presents an implementation of a continuous analytical model of GC (Graded-Channel) SOI nMOSFET using MATLAB. The MATLAB program is widely used in engineering applications due to its great flexibility to solve a set of linear or nonlinear equations. In this case, MATLAB is useful once this implementation requires a great number of equations. A comparison between the results of the simulations made from the implementation of this model to experimental measurements and results of MEDICI numerical two-dimensional simulator is performed, validating the proposed implementation.

## 1. INTRODUCTION

The Graded-Channel SOI MOSFET (GC SOI) is a new device [1] with an asymmetrical channel doping profile. The channel is divided in two parts: the first one is in the drain side, presents a low doping level and length $L_{LD;}$ the remaining part (source side) has the usual doping concentration and length L-$L_{LD}$, where L is the total length of the channel, as shown in figure 1.

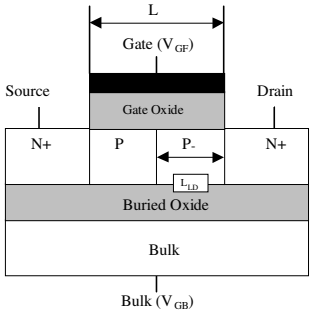


Figure 1 – Cross-section of the Graded-Channel SOI nMOSFET.

Previous works reported that GC SOI MOSFET can be interpreted as a series association of two SOI MOSFET transistors each representing one part of the channel, connected by an intermediate node [1]. This node represents the potential of the transition region between the different doping concentrations in the channel, which is previously unknown. To solve the set of equations that result from this interpretation, the use of iterative method is necessary, once two equations can describe the current that flows in the channel of the transistor.

The goal of this work is to implement a continuous analytical model of GC SOI nMOSFET using MATLAB [2] and validate this model through the comparison between its results and results of MEDICI numerical two-dimensional simulations and experimental measurements realized in manufactured transistors.

## 2. ANALYTICAL MODEL DESCRIPTION

The presented model is based in a linear relation between the inversion charge ($Q_{nf}$) and the front surface potential ($\phi_{SF}$) [3]. However, in a GC SOI transistor, that has two different doping levels, the surface inversion charge is divided in two parts. The surface inversion charge in turn is a function of the variation of potential in the interior of the channel (V(y)).

The drain current ($I_{DS}$) is expressed as a function of the inversion charges. Once in a GC SOI transistor the inversion charge is divided in two different parts, the drain current can be written as:

$$I_{DS} = \frac{\mu_{HD}.W}{L - L_{LD}} \left[ v_T \left( Q_{nf,HD_{L-L_{LD}}} - Q_{nf,HD_0} \right) - \frac{Q_{nf,HD_{L-L_{LD}}}^{\ 2} - Q_{nf,HD_0}^{\ 2}}{2.n.C_{oxf}} \right] \quad (1)$$

$$I_{DS} = \frac{\mu_{LD}.W}{L_{LD}} \left[ v_T \left( Q_{nf,LD_L} - Q_{nf,LDL-L_{LD}} \right) - \frac{Q_{nf,LD_L}^{\ 2} - Q_{nf,LD_{L-L_{LD}}}^{\ 2}}{2.n.C_{oxf}} \right] \quad (2)$$

where $\mu_{HD}$ and $\mu_{LD}$ are the mobilities of electrons in both parts of the channel; $v_T$ is the thermal voltage; $Q_{nf,HD}$ is the inversion charge in the conventionally doped region of the channel; $Q_{nf,LD}$ is the inversion charge in the low doped part of the channel; n is the body factor and $C_{oxf}$ is the gate oxide capacitance.

From these equations it is possible to interpret the presented model as a series association of two transistors, representing both parts of the channel, connected by an intermediate node. This node ($V_{tran}$) will be the drain voltage of the conventionally doped transistor and the source of the low doped one. $Q_{nf,HDL-LD}$ and $Q_{nf,HD0}$ are the inversion charges at the transition region of the channel and in the source end, respectively, obtained by solving the equation that describes the surface inversion charge with $V(y)=V_{Tran}$ and $V(y)=0$. $Q_{nf,LDL}$ and $Q_{nf,LDL-LD}$ are the inversion charges in the drain end and in the transition region for the low doped transistor, obtained by solving the same equation with $V(y)=V_{Tran}$ and $V(y)=V_D$, respectively.

## 3. IMPLEMENTATION STRATEGY

Since the drain current can be described through two different equations, (1) and (2) are equal and one can write:

$$I_{DS,HD} - I_{DS,LD} = 0 \quad (3)$$

where $I_{DS,HD}$ is the current drain obtained by solving equation (1) and $I_{DS,LD}$ is the current drain obtained by the equation (2). Then, we have an equation whose variable is an intermediate node of the channel ($V_{Tran}$). However, this variable is not easily isolated in this equation.

Therefore, we used a successive approximations method to locate the root of equation (3). Is previously known that $V_{Tran}$ is a value smaller than the drain voltage applied in GC SOI transistor ($V_D$). Thus, we assume $V_D$ as the initial value for $V_{Tran}$. Then, we calculate the result of the equation (3) and compare it with the allowable error. If the result were larger than the allowable error, $V_{Tran}$ is decreased and a new value from equation (3) is calculated. This algorithm is repeated until the convergence is achieved (result of equation (3) ≤ allowable error). The value of each decrease of $V_{Tran}$ is 0.5mV and the number of necessary iterations is variable. For simulations of GC SOI nMOSFET with $L_{LD}/L$=0.5, $V_{DS}$ = 0.1V and $V_{GF}$ = 3V, the convergence is achieved after less than 70 iterations; the smaller is $V_{GF}$ and the ratio $L_{LD}/L$, the smaller is the number of iterations necessaries to achieve the convergence.

## 4. RESULTS AND DISCUSSION

The proposed model implementation was first validated by a comparison to MEDICI numerical two-dimensional simulations, resulting in a good agreement. The comparison was made for GC SOI nMOSFETs with $L_{LD}/L$= 0.25 and 0.5, with $V_{DS}$ = 0.1V and

varying $V_{GF}$ from 0.5 to 3V to $I_{DS}$ x $V_{GF}$ curves, as shown in figure 2.

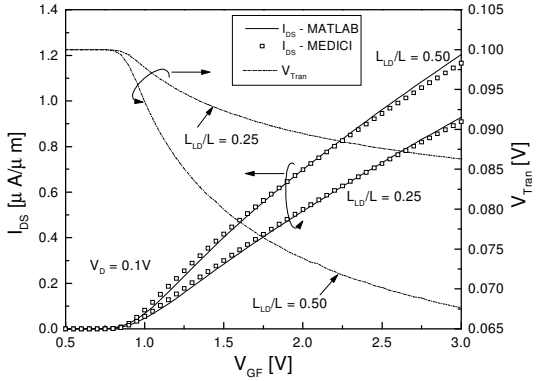


Figure 2 – Comparison between MATLAB and MEDICI simulated $I_{DS}$ x $V_{GF}$ curves. MATLAB simulated behaviour of $V_{Tran}$ x $V_{GF}$

Figure 3 shows the $I_{DS}$ x $V_{DS}$ curve for a gate voltage overdrive ($V_{GT} = V_{GS} - Vth$, where Vth is the threshold voltage) of 250 mV, obtained varying $V_{DS}$ from 0 to 2.0V.

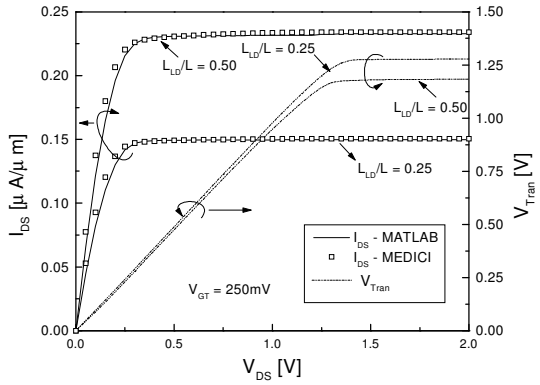


Figure 3 – MEDICI and MATLAB simulated $I_{DS}$ x $V_{DS}$ curves. MATLAB simulated behaviour of $V_{Tran}$ x $V_{DS}$.

The proposed implementation allows the observation of $V_{Tran}$, as presented in figure 2. It can be seen that $V_{Tran}$ remain almost equal to $V_{DS}$ up to the overall device threshold voltage is reached (around 0.8V in figure 2). For larger $V_{GF}$ there is a reduction of $V_{Tran}$ which is a function of $L_{LD}/L$: the larger is $L_{LD}/L$ the smaller is $V_{Tran}$. Figure 3 presents the MATLAB behaviour of $V_{Tran}$ varying the drain voltage ($V_D$). Due to an effective device channel length reduction there is a decrease in the intermediate node voltage ($V_{Tran}$) as indicated in figure 3.

As seen in figure 4, the proposed implementation also allows the observation of the voltage between drain and source ($V_{DS}$) for both transistors that represents each part of the channel, being $V_{DS,HD} = V_{Tran}$ and $V_{DS,LD} = V_D - V_{Tran}$.

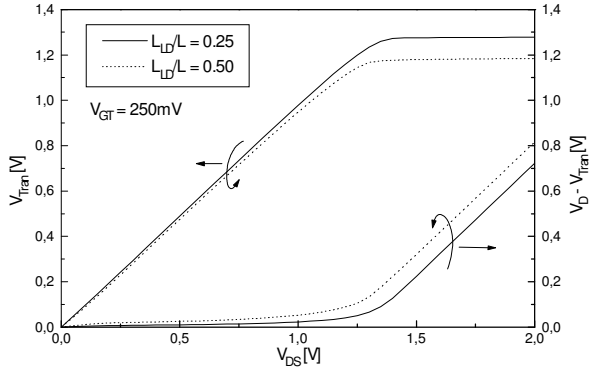


Figure 4 – $V_{Tran}$ and $V_D$-$V_{Tran}$ x VD curves, that represents $V_{DS,HD}$ and $V_{DS,LD}$

Afterwards, we compared the implemented continuous model with experimental measurements. Figure 5 presents the comparison between the results obtained for $I_{DS}$ x $V_{GF}$ (simulated with $V_{DS}$=0.1V) for GC SOI nMOSFET with $L_{LD}/L$= 0.25 and 0.5 and experimental measurements realized in manufactured transistors.

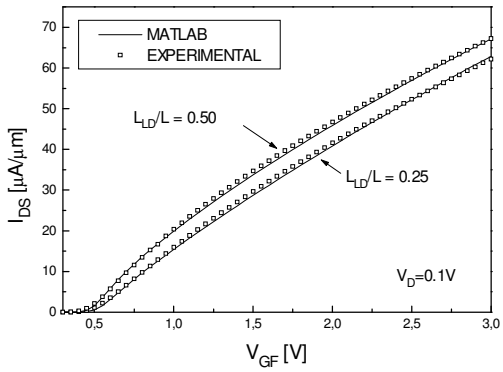


Figure 5 – Comparison between MATLAB simulated and experimental measurements for $I_{DS}$ x $V_{GF}$ curves.

In figure 6 is presented the $I_{DS}$ x $V_{DS}$ for a gate voltage overdrive $V_{GT}$ = 250 mV, obtained varying $V_{DS}$ from 0V to 3.0V.

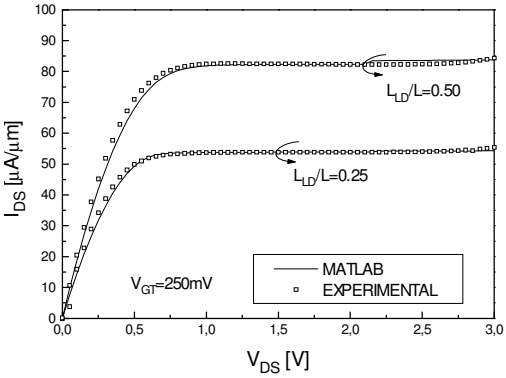


Figure 6 – Experimental measurements and MATLAB simulated $I_{DS}$ x $V_{DS}$ curves.

From the curves presented it is possible to verify the good agreement between the model equations solution and the numerical simulations and experimental results, validating the implementation described.

## 5. CONCLUSION

In this work we presented an implementation of continuous analytical model of GC (Graded-Channel) SOI nMOSFET using MATLAB. This model is equivalent to a series association of two conventionally SOI nMOSFET, each one with the characteristics of the part of the channel region that it represents, connected by an intermediate node. The comparison of the results of the implementation using MATLAB and results of numerical simulations and experimental measurements shows a good agreement.

## 6. ACKNOWLEDGEMENTS

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## 7. REFERENCES

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