FREQUENCY SYNTHESIZER FOR A SYSTEM-ON-CHIP RF TRANSCEIVER

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ABSTRACT

The design of a 0.35μm CMOS PLL-based Frequency Synthesizer for a RF transceiver is presented. The circuit operates in the 915-927 MHz range and was designed aiming reduced area and power consumption constraints.

1. INTRODUCTION

The Frequency Synthesizer is part of a system-on-chip transceiver. This system contains also a RISC processor, memory banks and digital and analog interfaces. The application proposed for the system is a node for a wireless sensor network operating in the 915MHz – 927MHz frequency range. Each node must be accessed remotely by a central station and have one year autonomy (powered by batteries) which demands power optimization. Communication between node and central uses 50KHz channels. The channel frequency is controlled by the processor and generated by the frequency synthesizer. The system employs a 0.35 micron double-poly, 4-metal CMOS technology (AMS), which is adequate for the proposed application.

2. PHASE-LOCKED LOOP SYNTHESIZER TOPOLOGY

The PLL synthesizer topology is shown in Figure 1. It is a dual-modululs prescaler with charge-pump loop filter. The 16 MHz input reference frequency is a external crystal-based oscillator. The PLL´s feedback network is composed by three frequency dividers (N, M, F) which determine the voltage-controlled oscillator (VCO) frequency according to equation 1 [3].

$$f_{VCO} = f_{ref} \times \left(M \times N + F\right) \qquad [1]$$

The phase-frequency detector (PFD) compares the reference frequency to the divided by the feedback network VCO frequency. The PFD provides a digital signal that is related to the phase and frequency differences of the input signals. The purpose of the charge-pump loop filter is to convert logic states of the phase-frequency detector into analog signals suitable for controlling the VCO frequency [1].

In this paper the voltage-controlled oscillator and the phase-frequency detector are developed and analyzed for the purposes of the system described in the previous section.

3. VOLTAGE-CONTROLLED OSCILLATOR

The VCO topology proposed is a inverter-based ring oscillator due to its programmable output frequency range and its smaller area when compared to other multivibrator oscillator topologies.

Two kinds of frequency control were studied:

a. A Voltage-controlled series resistor connected between each inverter stage, implemented with CMOS transmission gates [2]. In this paper, this VCO topology is referred as VCOTG;
b. A Voltage-controlled resistor connected with a capacitor, between each inverter stage , in order to provide an incremental time constant RC [4]. In this paper, this VCO is referred as VCORC.

In both cases, the VCO is a five stage inverter-ring oscillator with their frequency control given by varying the RC time constant between each stage. Figure 2a shows one stage of VCOTG and Figure 2b shows one stage of VCORC. Both topologies were designed and simulated with SPICE . The time responses of both types of VCO are similar. Then, for illustration purposes, only the response of the VCOTG was shown, Figure 3. Results for both kinds of ring oscillator are summarized in Table 1.

4. PHASE-FREQUENCY DETECTOR

A digital phase-frequency detector (PFD) is commonly used in PLL circuits because of the ease of implementation and the built-in frequency detector feature for low frequencies [1].

For the circuit in Figure 1, the topology used for this block is a standard PFD developed by Motorola [1]. This circuit is designed to lock with null phase difference. The implementation uses basic NAND and NOT gates as is shown in Figure 4.

The circuit was simulated, Figure 5, and it worked as related in the references [1,3].

5. DISCUSSION

Based on the results summarized in Table 1, the adequate oscillator to the proposed synthesizer is the VCORC. This VCO is the only one capable of synthesizing the required frequency range. In addition it needs only one control signal which can vary from VDD to VSS and can be connected directly from the loop filter output. The VCOTG frequency is highly limited by the series resistor connected between each inverter stage.

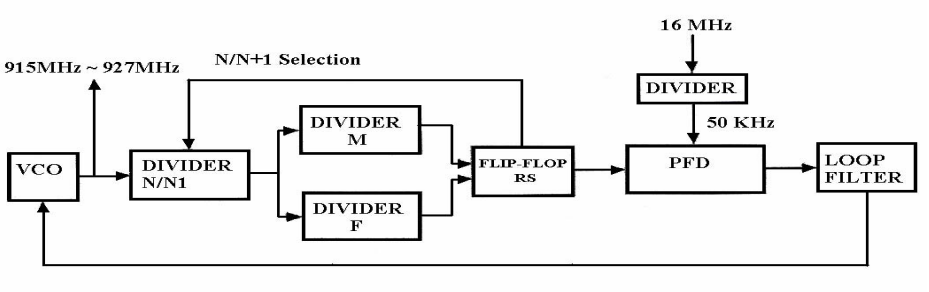
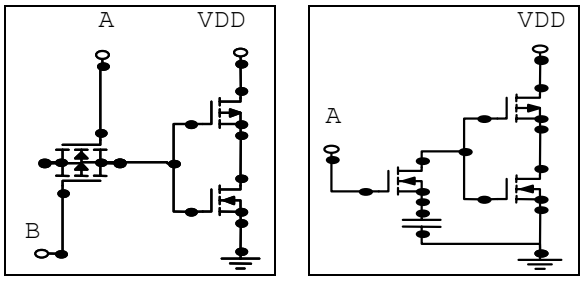


Figure 1 – Dual modulus prescaler PLL Synthesizer



(a) **(b)**

Figure 2 – One stage of VCOTG (a) and VCORC (b)

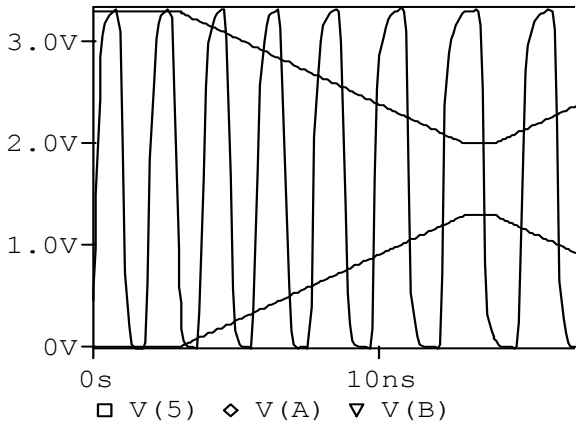


Figure 3 – Time response of the VCOTG

The implemented PFD showed desirable time response with a differential output that results in lower power consumption

6. CONCLUSION

The voltage-controlled oscillator is the main block from a frequency synthesizer and it was developed in this work. A phase-frequency detector was simulated and presented a satisfactory behavior. The next step for the synthesizer design's conclusion will be the loop filter's conception.

Table 1 – Comparison between VCOTG and VCORC

Characteristic	VCOTG	VCORC
tuning range	360 – 540MHz	886 – 1027MHz
gain	13,8MHz / 100mV	4,2MHz/100mV
area	80μm^2	70μm^2
power	2,6mW	2,43mW
references	[2]	[4]
frequency control	two complementary signals	one signal

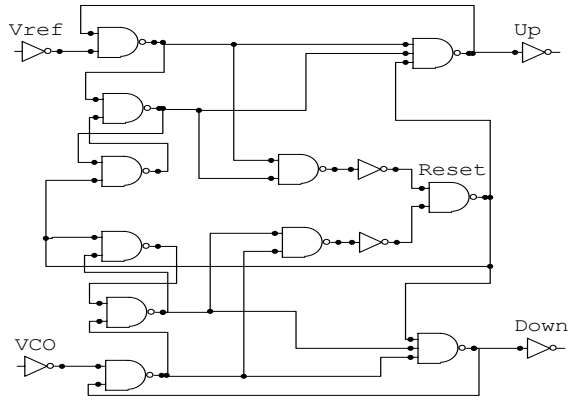


Figure 4 – Digital PFD topology

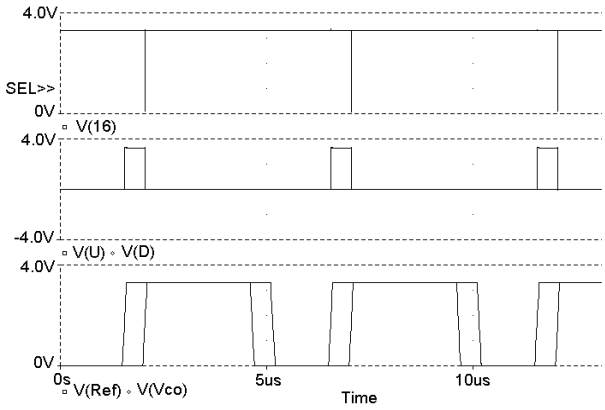


Figure 5 – Time response of the PFD

7. REFERENCES

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