ON-CHIP TEST CIRCUITRY FOR FULLY-DIFFERENTIAL STRUCTURES

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ABSTRACT: An on-chip circuitry for the experimental characterization of fully-differential structures is presented. An operational amplifier with a Class-AB output stage was used as a basic cell to implement the building blocks. PSPICE simulation attests the theoretical analysis. Circuits were prototyped according to a 0.35µm CMOS process. For symmetrical supply voltages of ±2.5V and bias current of 100µA, main experimental results are GBW = 25MHz, CMR = [-1.2V, 1.2V], settling time (1%) = 120ns and SR = 50V/µs.

1. INTRODUCTION

Fully-differential structures are key parts to the design of low-voltage analog integrated circuits, as signal swinging is doubled with respect to singled-ended approaches. However, to properly characterize such structures, it is essential to generate balanced input stimuli and to process differential outputs. Off-chip circuitry performing these functions allow a fast test cycle, although suffering from undesired effects: 1) the limitation of the frequency response due to commercial components and stray connections; 2) the meaningful mismatching between positive and negative paths of the balanced signal and 3) an increase of the pick-up noise. As a consequence, on-chip testing appears as a better solution to handle fully-differential circuits.
The paper is organized as follows. Circuit design and simulation is presented in Section 2, followed by experimental results in Section 3. Concluding remarks are summarized in Section 4.

2. CIRCUIT DESIGN AND SIMULATION

Figure 1 displays the block diagram of the implemented circuits. It consists of a differential-generator (DG) to supply the balanced stimulus to the device under test (DUT) and a differential amplifier (DA) that converts the DUT outputs to a singled-ended signal. The opamp-based schematics of DG and DA blocks are illustrated in Figure 2 and 3, respectively.

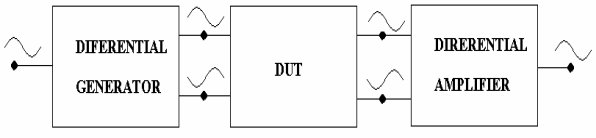


Figure 1 – Block Diagram of the developed System

The full schematic of the opamp is shown in Figure 4. The circuits were sized and integrated in accordance with a 0.35µm n-well CMOS process, symmetrical power supplies of ±2.5V and a bias current I_{BIAS} = 100µA. Process parameters are typically V_{THN} = 0.50V, V_{THP} = -0.60V, γ_n = 0.58V$^{1/2}$, γ_p = 0.45V$^{1/2}$, μ_n = 385cm^2/Vs, μ_p = 130cm^2/Vs and C_{ox} = 456nF/cm^2.

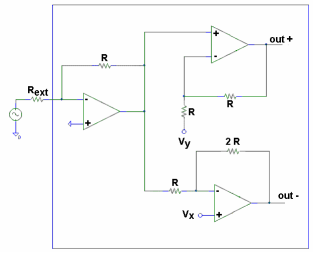


Figure 2 – Differential Generator

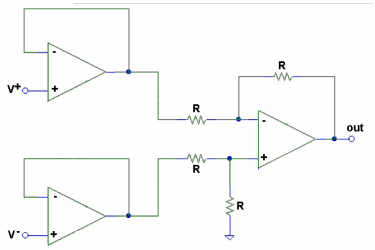
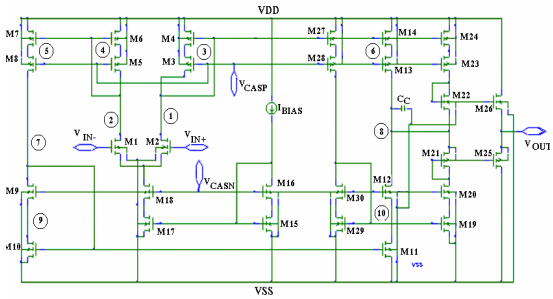


Figure 3 – Differential Amplifier



4 – OTA with Class-AB output stage

Simulation results were obtained with PSPICE 9.2 and Bsim3v3 models. From the simulated open-loop frequency response of the designed opamp shown in Figure 4, one has GBW = 25MHz, A_{V0} = 70dB and ϕ_M = 45º, for a resistive/capacitive load of 100kΩ and 15pF. Figure 6 displays a settling time of around 100ns (1% within final value) and Figure 7 shows a slew-rate of 55V/µs. The transistor sizing dimensions of the amplifier is listed in Table I.

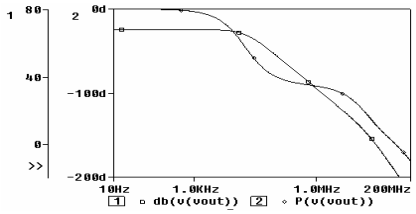


Figure 5 – Opamp open-loop frequency response

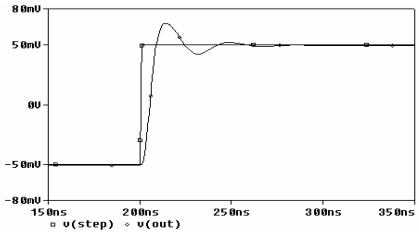


Figure 6 – Opamp settling-time response

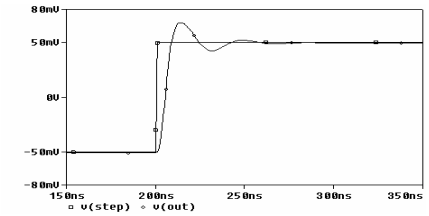


Figure 7 – Slew Rate response

W / L	MOS	W / L	MOS
100 / 1	$M_{1,2}$	50 / 1	$M_{15\text{-}18}$
20 / 1.4	$M_{3\text{-}6,\ 9\text{-}12,\ 23,\ 24,\ 27,\ 28}$	50 / 0.4	M_{22}
10 / 1.4	$M_{19,20,29,30}$	100 / 0.4	M_{21}
60 / 1.4	$M_{7,8,13,14}$	200 / 0.4	M_{26}
10 / 2.5	$M_{7,8,13,14}$	400 / 0.4	M_{25}

Table I – Opamp transistor draw-sizing

3. EXPERIMENTAL RESULTS

The designed circuits were prototyped using a 0.35µm CMOS process. The die photography is shown in Fig. 7. Experimental results are presented in figures 8-9.

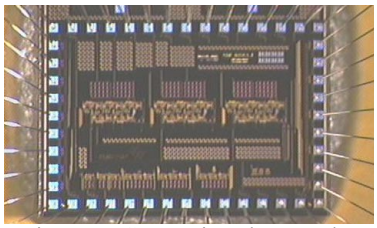


Figure 7 - CHIP Microphotography

The experimental results are in accordance with theoretical and simulation analysis. Circuits can operate within acceptable levels of distortion up to 10MHz, for low amplitude signals (<100mV). At a maximum value of 3MHz , an output swing of ± 1.2V is reached. A 20%-deviation in the settling time response (120ns) with respect to simulation value (100ns) can be attributed to a finite inclination of the practical step input. Table II summarizes the simulated and practical values the amplifier main parameters.

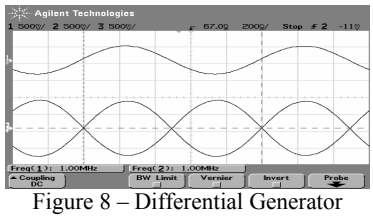


Figure 8 – Differential Generator

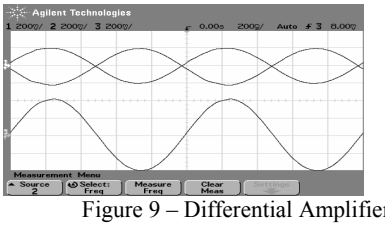


Figure 9 – Differential Amplifier

	Simulation	Experimental
GBW	25 MHz	23MHz
Settling Time	100ns	120ns
CMR	[-1.2V,1.2V]	[-1.2V,1.2V]
Slew Rate	55V/µs	50V/µs

Table II – Opamp simulated and measured parameters

4. CONCLUSIONS

An on-chip circuitry for the experimental characterization of fully-differential structures was implemented on a 0.35µm CMOS process. A differential-generator to supply the balanced stimulus to the device under test (DUT) and a differential amplifier that converts the DUT outputs to a singled-ended signal was developed. An operational amplifier with a Class-AB output stage was used as a basic cell to implement the building blocks. Poly resistors are used to build up closed-loop configurations. Experimental results agree with theoretical and simulation analysis. For symmetrical supplies of ±2.5V and bias current of 100µA, the opamp measured parameters are GBW = 25MHz, CMR = [-1.2V, 1.2V], settling time (1%) = 120ns and SR = 50V/µs. The circuits operate within acceptable distortion up to 10MHz for low-amplitude signals (<100mV) and, for a maximum output swing of 1.2V, maximum operating frequency is 3MHz.

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