A Bandgap Reference Circuit in 0.35µm CMOS Technology with Trimming Array

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ABSTRACT

This paper describes the design of a bandgap reference, implemented in 0.35µm CMOS technology. The circuit generates a 1.223V reference voltage and has a maximum temperature coefficient of 40ppm/ºC. It can operate with supply voltages between 3.3V and 2.3V and temperatures between -50ºC and 150ºC. It has a PSRR of 40dB under normal operating conditions. The design was implemented aiming at maximum matching of its components and it includes a trimming array for adjusting the temperature coefficient.

1. INTRODUCTION

One of the essential building blocks of most analog circuits is a stable voltage reference, which should exhibit little dependence on supply and process parameters and a minimum dependence on temperature.

As a well-established reference generator technique, the bandgap reference is most popular for both Bipolar and CMOS technologies. The bandgap reference used in diverse application is based on the idea of Hibilber in 1964 [1].

2. CIRCUIT DESCRIPTION

The principle behind the bandgap reference is illustrated in Fig 1. A voltage Vbe is generated from a pn-junction diode having a temperature coefficient of approximately –2mV/°C. Another circuit generates a thermal voltage (Vt =k.T/q) where, k is Boltzmann's constant, T is the absolute Temperature and q is the electron charge, that has a temperature coefficient of +0.085mV/°C. If the Vt voltage is multiplied by constant K and added to the Vbe voltage, then the output voltage is given as:

$$V_{REF}=V_{BE}+KV_t \qquad (1)$$

Differentiating eq. 1 with respect to temperature that should theoretically give zero temperature dependence [2].

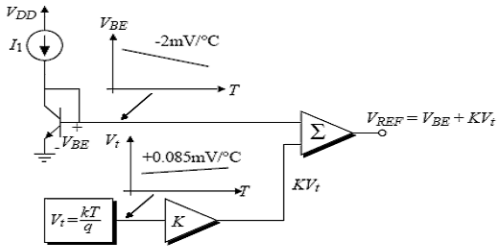


Fig 1 - General band-gap reference principle.

3. CIRCUIT DESIGN

The architecture used in this work is shown in Fig. 2. In this topology, the MOS transistors are utilized as current mirrors only, as the Q3 and Q4 pair. Considering that the transistors Q1 and Q2 also have the same aspect ratio and the same current, both V_{GS} are the same. Thus, the voltage across R1 can be found using the following equation:

$$V_{R1}=V_{EB6}-V_{EB7,8}=\frac{kT}{q}\ln\left(\frac{I_{C6}}{I_{C7,8}}\right)=\frac{kT}{q}\ln(2) \qquad (2)$$

On the other hand, under constant current, the potential of a bipolar junction (i.e. the Vbe of a BJT, Q9 in that case) has a thermal behavior that can be described by:

$$V_{EB}(T)=V_{EB0}-\alpha T+f(T) \qquad (3)$$

Where VEB0 corresponds to VEB in a reference temperature, α varies from 2.0 to 2.5 mV/°C and f (T) is a second order effect with minor influence in the result, resulting in a VBE behavior almost linear with the temperature.

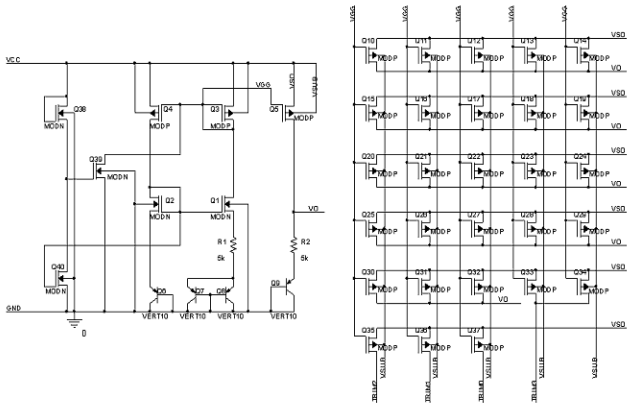


Fig 2 - Circuit topology including the Trimming Array

3.1 Components Sizing

Component sizing was done taking matching parameters from [3] into account. Table 1 presents the final sizing of the components (vertical BJT, MOSFET and Resistors) of the circuit, which are large to minimize process variations.

Table 1 - Component dimensions - BandGap

	Q1,2	*Q3,4*	*BJT's*	*Q5, 10,35*	*Q36*	*Q37*	*Q38*	*Q39, 40*	*R1*	*R2*
W(μm)	80	70	32.6	20	10	5	1	10	10	10
L(μm)	80	70	μm^2	20	20	20	80	1	1K	1K

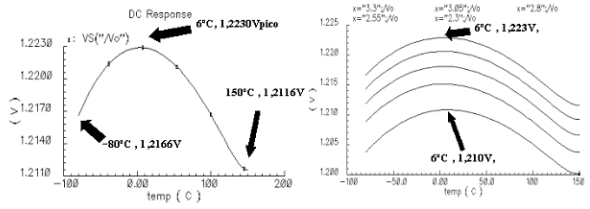
3.2 Trimming Array

In the proposed topology[4], adopted trimming as strategy to set the temperature for which zero temperature drift is obtained. It can be made by adjusting the relation between the current that flows through R1 and through R2. Consequently, we are able to adjust the thermal stability of the circuit. For this purpose, an array of 4 MOS transistors was included with W sized in 2X steps (2W, W, W/2 and W/4), with the terminals of gate (G) and source (S) connected in parallel to Q5 and having the drain (D) terminals connected to four additional PADs. Thus, the current through R2 can be adjusted in up to 16 levels, proportionally to the current that flows through R1 by selectively connecting these 4 PADs to the Vo node.

4. CIRCUIT ANALYSIS

4.1 Temperature Variation

The curve in Figure 4a presents the output voltage Vo as a function of the temperature, and the curve in figure 4b shows Vo as a function of Vdd voltage in the interval 2.3 to 3.3 V, in the same temperature range.



4a 4b

Fig 4 - A tipical Bandgap curve

4.2 Temperature Variation ***versus*** Trimming Adjustment

Fig. 5 shows the circuit response considering all possible combinations for the input trimming.

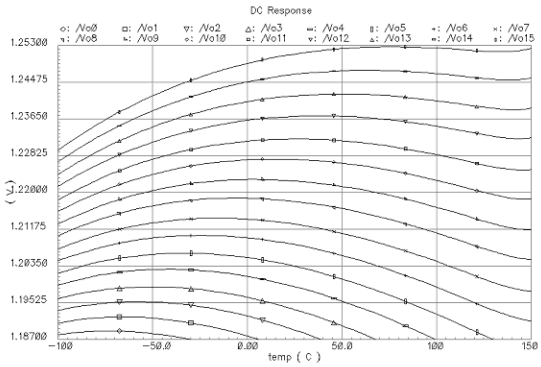


Fig 5 - All possible combinations of trimming

4.3 Power Supply Rejection Ratio (PSRR)

Fig. 6 shows simulation of PSRR vs. frequency for the circuit. To simulate this effect, an AC voltage source in series to VDD was used to simulate supply noise. The result shows a PSRR of -40dB below 200KHz.

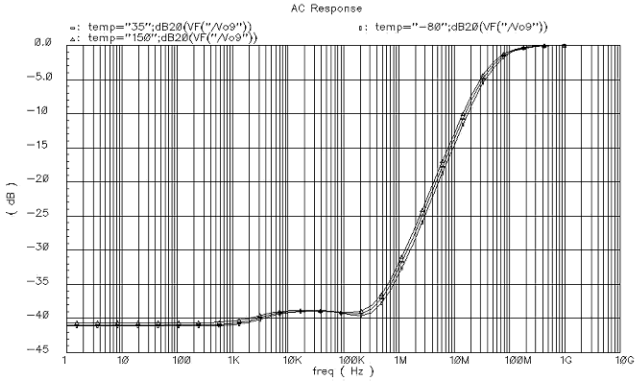


Fig 6 - PSRR simulation

5. LAYOUT

Fig. 7 shows the layout of the circuit. The chip occupies a total area of 350 x 400μm^2 in CMOS 0.35um.

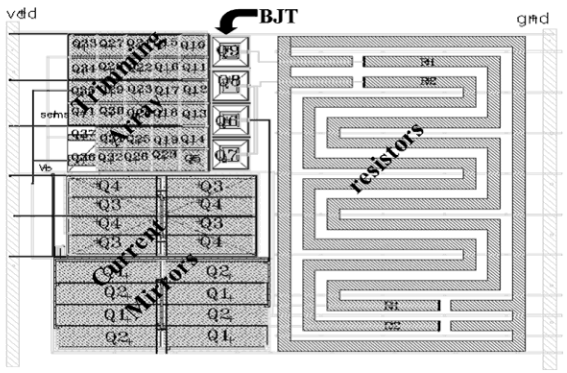


Fig. 7 - Complete layout

6. CONCLUSION

A bandgap reference circuit has been designed, with a thermal drift of 40ppm/°C in the operation region and variation of 1%~2% of Vo/per Volt of Vdd. A considerable silicon area was occupied, because of the accurate optimization required to match the components of this circuit. The circuit fabrication is underway in the AMS foundry.

7. REFERENCES

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