

Design of a 4-bit Processor for Evaluating of the E/D nMOS Technology from CCS/UNICAMP

Felipe R. Schneider, Renato E. B. Poli, Daniel Barden, Davi K. Leonel, Diogo A. Fiorentin, Francisco M. Trindade, Fernando S. de Vasconcellos, Mário C. de B. Osório Neto, Renato P. Ribas

Instituto de Informática – UFRGS
 Av. Bento Gonçalves 9500, CEP 91501-970 – CxP 15061
 Porto Alegre, RS – Brazil
 {felipers, rpribas}@inf.ufrgs.br

ABSTRACT

This paper presents the design of an ASIC conceived for a 4-bit processor through the use of a 5 μm E/D (Enhancement/Depletion) nMOS process from CCS/UNICAMP. The goal of such work is to evaluate the potential of this technology for both educational and research purposes. The fabrication is going on.

1. INTRODUCTION

It will be presented in this paper the chip design of a processor architecture so called Neander [1]. Neander is a didactic and virtual architecture known by its software emulator, which is used to teach computer architecture and assembly languages to undergraduate students. The main goal of this project is to use the processor construction as a case of study for evaluating the technology process developed at the Semiconductor Components Center (CCS) from UNICAMP, Brazil.

This paper is organized as follows: In Section 2 we discuss some design issues regarding to the fabrication technology. In Section 3, the processor architecture is briefly introduced. Some results obtained during the project are presented in Section 4. Finally, conclusions about this work are given in Section 5.

2. TECHNOLOGY PROCESS

The fabrication process available to build the chip is an E/D (Enhancement/Depletion) nMOS technology with only one layer of metal. The minimum channel width used in this project was 5 μm , but recent research at UNICAMP achieved 1.7 μm [2].

As there is no polysilicon layer available to build the transistors gates, the metal layer was employed for both interconnection and gate construction. To build the transistors gates, regions of thinner oxide are defined in the layout masks.

Hence, the limitation in using just one layer of metal and the absence of polysilicon implied in difficulty of routing: it's not possible to cross metal segments if one don't want contact between them. The solution for such problem was to route for small distances using the same diffusion applied in the construction of enhancement region (Fig. 1).

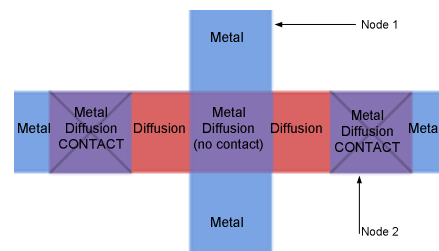


Fig. 1 – Interconnection crossing.

The CCS process, nowadays, is mainly used as a microfabrication research platform. So, to study the potential for the didactic employment of such technology, a class of students chose to develop an ASIC of a simple processor architecture using the CCS process.

3. PROCESSOR ARCHITECTURE

The original version of Neander is an 8-bit word length processor architecture. In [3] the chip design of such processor, using a CMOS 0.35 μm process is presented.

However, due to the limitations of the available technology and in order to achieve the conclusion of the design on a short time, the architecture was adapted to a 4-bit word length processor. Table I presents the set of instructions implemented and Fig. 2 shows a diagram of the Neander architecture.

Table I – Neander's instruction set.

opcode	instruction	#op.	function
0001	LDA <i>opl</i>	2	ACC \ll <i>opl</i>
1001	ADD <i>opl</i>	2	ACC \ll <i>opl</i> + AC
0011	OR <i>opl</i>	2	ACC \ll <i>opl</i> OR ACC
1101	NOT <i>opl</i>	1	ACC \ll NOT ACC
0000	STA <i>opl</i>	2	[MEM: <i>opl</i>] \ll ACC
0010	JMP <i>opl</i>	3	PC \ll <i>opl</i> : <i>op2</i>
0100	JZ <i>opl</i>	3	If ACC = 0 then PC \ll <i>opl</i> : <i>op2</i>
1011	AND <i>opl</i>	2	Acc \ll ACC AND <i>opl</i>

4. RESULTS

To go from behavioral to physical design the bottom-up methodology approach was employed. It implies that basic cells had to be developed in order to generate more

complex blocks until achieve the final chip. The layout of one of these cells, a NOR4, is presented in Fig. 3.

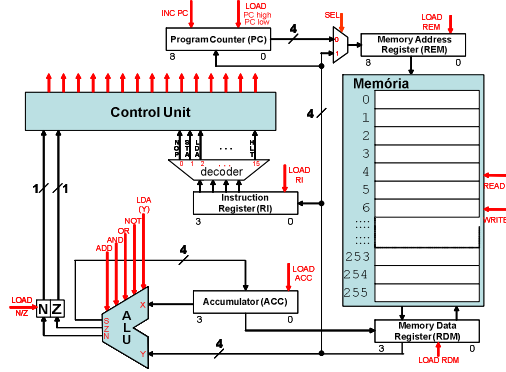


Fig. 2 – Neander architecture.

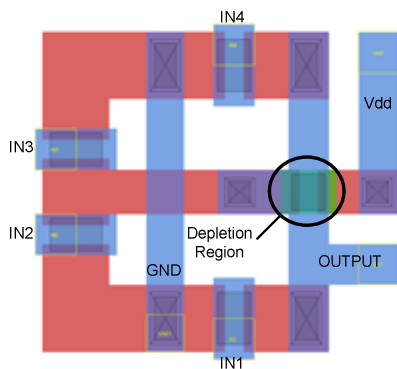


Fig. 3 – NOR4 layout.

The layout extraction, is not present in the design flow because the extraction rules in technology file available were not set up. The addition of such extraction parameters to the technology file will be certainly an important job to be made in future work.

Due to the limitations of the fabrication process, inexperience of engineering students and thinking on increasing the yield, it was used four chips to embody the whole project. One of them, the Neander’s control unit chip, is presented in Fig 4. These chips were made in such manner they could be individually tested after their fabrication: additional pads for intermediate signals were added inside them. Table II presents the dimensions and number of devices of all chips.

Another consideration made at design time was the need of a memory for data and instructions. Therefore, the entire project was done considering the use of available commercial RAM memories.

Table II – Dimensions and number of devices of all chips.

Chip	Size (mm x mm)	#transistors
Control Unit	4.04 x 4,12	430
Arithmetic and Logic Unit	4.03 x 4,12	330
Register (ACC, REM, RDM or RI)	3.55 x 2,82	624
Program Counter	2.78 x 1.88	509

The boundary pads used are very simple, and they have no kind of protection: the input and supply pads use only wire to connect to internal logic and the output pads have an ordinary buffer.

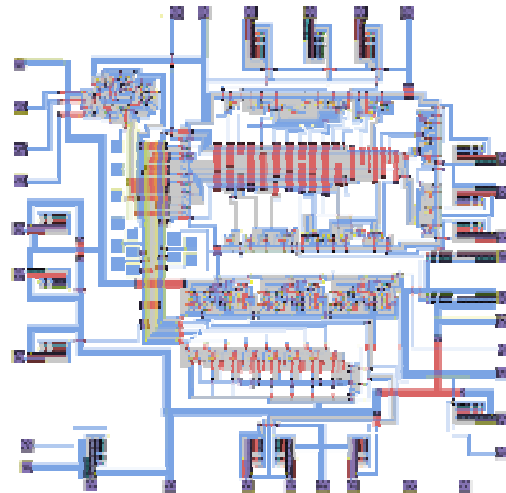


Fig. 4 – Processor’s Control Unit chip layout.

The electrical simulation of the cells was done using SPICE level 3 model parameters provided by CCS. Unfortunately, due to incomprehensive troubles, it was not possible to simulate or estimate performance parameters for circuits larger than a basic logic gate. The Table III presents, just for a matter of illustration, comparative delay estimation for the NAND3 logic gate used in the Neander design.

Table III – NAND3 performance estimation.

	t_D	t_{LH}	t_{HL}
CCS 5 μ m	248,75 ns	464,22 ns	271,61 ns
AMIS CMOS 0.5 μ m	0,256 ns	0,503 ns	0,380 ns

5. CONCLUSIONS

In this paper the project of a 4-bit processor had been presented. It was done aiming the evaluation an nMOS technology process developed in CCS/UNICAMP, Brazil. Although this process is far from state-of-the-art, it is believed that such technology can be a valuable platform to academic students to learn and research in the field of microelectronics, where performance issues are not so important.

The CCS reports that there is no project as big and complex as the Neander processor fabricated in that center until now. The project presented here was entirely designed by undergraduate students and it took, approximately, 2 months to be concluded. It is also emphasized that almost all the CAD tools used to accomplish this project were free software. The chips are under fabrication.

6. REFERENCES

- [1]Weber, R. F. *Fundamentos de Arquiteturas de Computadores*. Série Livros Didáticos de Instituto de Informática da UFRGS. Ed. Sagra Luzzatto, Porto Alegre, 2000.
- [2]Manera, L. T. *Determinação de Regras de Projeto de Simulação de um Processo nMOS para Fabricação de Circuitos Integrados*. Dissertação de Mestrado, UNICAMP. Campinas, julho de 2002.
- [3]Poli, R. E. B. et al. *Neander, 8-bit processor design flow*. Student Forum. Porto de Galinhas, 2004.