Design, Implementation and Test of a 64 bytes SRAM using a CMOS technology

Paulo F. Butzen, Rodrigo Boccasius, Marcel F. Almeida, Renato P. Ribas

Instituto de Informática – UFRGS
CxP.15064, CEP 91501-970 Porto Alegre, Brazil
{pbutzen, rboccasi, almeida, rpribas}@inf.ufrgs.br

Abstract

This work presents the design flow of a 64 bytes SRAM memory circuit, including the architecture conception, the chip layout drawing and testing. The fabrication of the chip was possible thanks to the MOSIS educational program. The processor was conceived using the AMIS 0.5µm technology process. The whole circuit was designed with free CAD tools: Magic and Spice Opus. Decign methodology, logic and electrical circuit and testing issues are considered on this work.

1. Introduction

A memory is a device able to store and recover information previously stored. This device has a high importance in computational systems. Random access memories are a type of semiconductors memories and are divided in dynamic and static.

This work presents a description of the activities developed during the design of a 64 bytes SRAM memory chip projected to be used as the memory of a hypothetical processor developed in this university and used in several computers architectures disciplines.

The objective of this work with the project of a memory is besides studying the diverse implementations of this structure, also to study, to apply and to validate diverse techniques of simulation, layout and test.

Using the established accord between the UFRGS and the MOSIS educational program, the fabrication of integrated circuits designed by undergraduate students of this university was made possible. The project used only free design tools. For electrical design Spice Opus® [1], and for the layout conception was used Magic [2].

2. Memory Architecture

Three blocks of different devices form basic memory architecture. The first one are elements responsible for the decoding of accessed address. In this design columns and row decoders form this group, but in larger memory chips, usually there are another devices to multiplex the IO pins that choose the memory address. The second block is formed by memory cells (or SRAM bits) that are capable of storing the content of a data bit. There are different designs of memory cells in literature [4] [5]. In this design it was used a static memory cell without any kind of pre-charge. The third block of devices is formed by elements that are responsible for the shipment of the data from the cell selected to the interface with buses and amplifiers. In this design, buses without pre-charge were used together with sense amplifier that helps the IO pin driven.

From the logical elements that constitute the memory chip designed two elements are crucial and represents the most performance influence: the memory cell, because it is copied several times in the chip and defines the memory byte size, and the sense amplifiers, because it helps the driven of the bus that connect a number of cells avoiding that one single cell drives a capacitive bus.

Memory Cell - The static memory cells are formed by two invertors in ring connected to a bus through binding transistors enabled by the signals of line and column selection. A line of data and another line of data inverted form the buses. This type of linking is used to prevent electric problems. The schematics diagram of a memory cell can be observed in figure one.

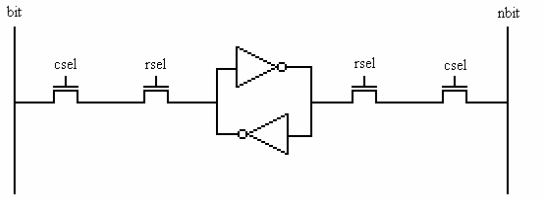

Fig. 1 – Memory cell schematics

Figure 2 shows the memory cell layout used in this design. The cell internal routing and the voltage lines uses poly and metal-1 layer so the inputs can be connected using metal-2 layer.

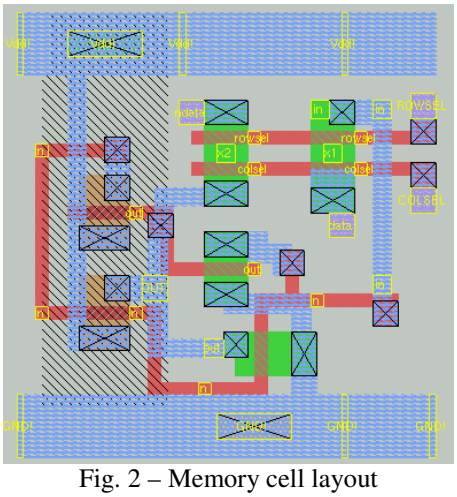

Fig. 2 – Memory cell layout

The memory cells are grouped in a matrix disposition, forming a bank of cells. A bank of cells is a symmetrical structure that groups the content of a data bit for all the possible memory addresses.

Sense Amplifier - A bank of cells is formed by memory cells hardwired in data buses. To prevent that a cell formed by only two as little as possible invertors needs to electrically load capacitive buses that is connected to many other cells it is necessary to use sense amplifiers. These amplifiers are amplifiers specialized in voltage difference between two signals so they can avoid the discharge of the cell driving the data bit with a little voltage supplied by the cell. In this design the sense amplifier were connected at each group of eight cells.

3. Results

The memory layout design was developed under the MOSIS CMOS process rules. The technology process was the AMIS C5F/N. It is a 0.5 micron process with three metal layers. The chip area was limited to 2,5mm x 2,5mm by the educational program. The entire rules and other information can be obtained in [3].

The final chip area was 6,25 mm^2 with 24 IO pins. Both constraints were determined by MOSIS. The chip design was finished with 5084 transistors, with 512 memory cells and 64 sense amplifiers. The micro-photo of the final circuit can be observed in figure three.

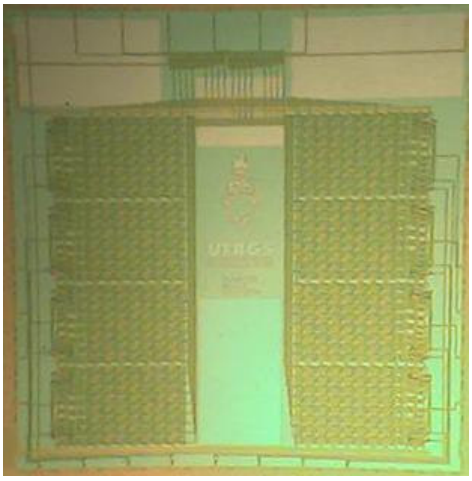

Fig. 3 – Micro-photo of the final circuit

The memory layout is a regular and symmetrical structure composed by eight banks of cells connected to the output pins. The area was not full occupied by the design because the area doubles for each bit increased in the address wide.

4. Test

The test of the memory was divided in two parts. The first one was the visual inspection of the circuit, in which finds manufacture defect as presented in figure 4.

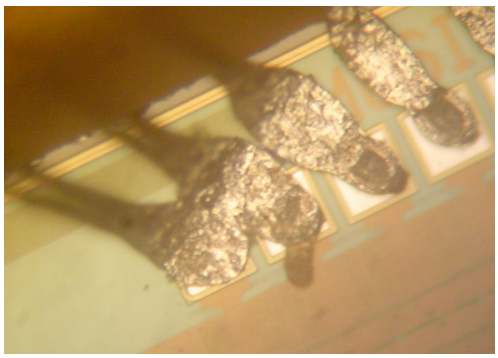

Fig 4 – Manufacture defect

Second it was the application of test vectors that would validate the circuit. In this second part of the tests problems had been found that had resulted in the detection of an error in PADs project, that they make impracticable its functioning.

5. Discussion

This work was important for providing to the undergraduate students the experience to participate of the complete flow of development of an integrated circuit. Many of microelectronics concepts are revised and others were learned.

A fault in the validation of the final layout, had the limitations of the used tools, and the use of a PAD library without the correct understanding of the functioning for the designers, allowed the existence of a project error that disable the functioning of circuit.

In circuit test, the visual test revealed as important as the functional test as shown in the detention of a manufacture defect.

6. Conclusions

This work presented a description of a 64 bytes SRAM design project flow developed by undergraduate students. The knowledge of the complete flow of the CI conception makes possible a great learning for the students.

From the detected error, the circuit is being re-designed. Other circuits also are being developed for students based in this initiative.

7. References

[1] Buermen, A. et al. Spice OPUS Homepage. http://www.fe.uni-lj.si/spice/welcome.html. CACD Group, 2002.

[2] Mayo, R. N. 1990 DECWRL/Livermore Magic Release. Western Research Laboratory. California, USA, 1990.

[3] MOSIS homepage. http://www.mosis.org.

[4] Weste, N., Eshraghian, K. Principles of CMOS VLSI Design. Addison-Wesley, 2nd edition, 1993.

[5] Rabaey, Jan, Digital Integrated Circuits, Prentice Hall, 1996.

[6] Butzen, Paulo F. Teste e caracterização de ASICs implementados na tecnologia AMI 0.5µm CMOS. Projeto de diplomação. 2005.