STUDY AND DESIGN OF A CMOS VOLTAGE CONTROLLED OSCILLATOR

Gustavo Gouvea Slade, Nobuo Oki, Vlademir J. S. Oliveira
Departamento de Engenharia Elétrica, Universidade Estadual Paulista
Caixa Postal 31, CEP: 15385-000 - Ilha Solteira - SP - Brasil

ggslade@aluno.feis.unesp.br,nobuo@dee.feis.unesp.br

ABSTRACT

A CMOS voltage controlled ring oscillator with quadrature output is presented. The circuit is designed in a 0.35µm CMOS process and 3V supply. The VCO has a tuning range of 690MHz to 1.15 GHz.

1-INTRODUCTION

The oscillators are important parts of many electronic systems and a lot of applications in electronics require that oscillators be tunable. These circuits are known as voltage controlled oscillators (VCO). They are widely used in applications such as*: phase locked loops* (PLLs), frequency (de)modulators, frequency synthesizer, and timing recovery circuits. [1].

A CMOS voltage controlled oscillator can be design using ring, relaxation, or LC oscillator. Ring oscillators are widely used, although with performance limitations, they offer low cost and they are easily implemented in standard CMOS technologies [2].

An odd number of inverters in a closed loop is called ring oscillator. The simplest ring oscillator is constructed with three inverters in a closed loop. This circuit, and all structures of ring oscillators, require both positive and negative feedback to operate correctly. Negative feedback is needed under DC conditions to allow the ring self-bias. On the other hand, positive feedback occurs as the phase shift of each stage increases with frequency. When the total phase shift around the closed loop reaches 360º and if the gain is greater than unity, the circuit oscillates (Barkhausen criteria). Under these conditions the closed loop gain of the ring is infinite. Therefore any signal introduced into the system, that contains energy at the frequency where the Barkhausen criteria is satisfied, will be amplified until nonlinearity limits it. The result is steady oscillation [3-4].

The normal behavior of oscillators with an even numbers of inverters is to not oscillate, although if it is biased properly, the even number of inverters can provide enough phase shift to facilitate positive feedback [4].

2-PROPOSED RING OSCILLATOR DESIGN

The configuration presented in figure 1 consists of four current starved inverters and two pairs of complementary devices used to couple the output of every other stage. In this way, the proposed oscillator can also be considered a two-stage differential design [4].

The configuration has the following characteristics: simple circuit, an even number

of stages produces differential operation and providing quadrature signals.

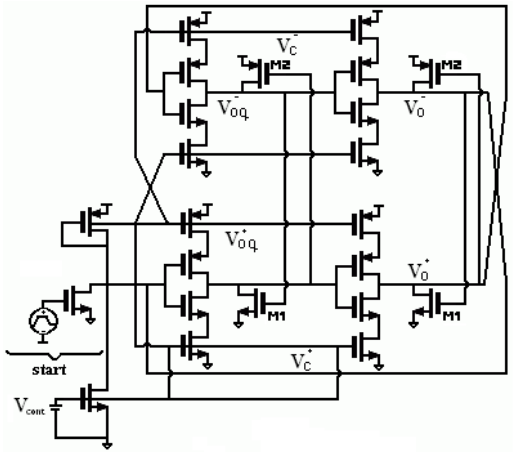

figura 1: Proposed ring oscillator design

3-SIMULATION RESULTS

The circuit was simulated using the PSPICE with 0.35-µm n-well CMOS BSIM3v3 parameters and 3 V supply voltage.

In the bias circuit in the figure 1, a current mirror was used, which is compound by one PMOS and one NMOS transistor that provide a negative feedback for output amplitude control [2].

The transistors aspect ratio used in this design are listed in Table 1. The output of the simulation is presented in figure 2.

Once, SPICE doesn't shape the device own noises, in the circuit illustrated in figure 1 a start system was used to get the simulations (illustrated in the same figure).

Table 1

Transistor	W/L (µm/µm)
M_1	1 / 0.8
M_2	20 / 0.8
Others NMOS	4 / 0.5
Others PMOS	20 / 0.5

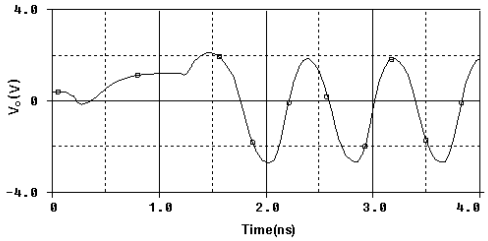

figura 2: Simulation resulting

The circuit presented a tuning range of 690MHZ, on 1.8V to 1.15GHz, on 3V.

4- CONCLUSION

It is presented a CMOS voltage controlled ring oscillator with four current starved inverters. The maxim frequency is 1.15GHz, what is useful in some applications. The next steps of the work consists of improve the circuit design and making its layout.

5 - ACKNOWLEDGMENT

This work was accomplished with the support of the National Council of Scientific and Technological Development – CNPq/PIBIC - Brazil.

6 - REFERENCES

[1] S. L. J Gierkink and E. van Tuij, "A Coupled Sawtooth Oscillator Combining Low Jitter with High Control Linearity", IEEE Journal of Solid-State Circuits, vol. 37, n. 6, jun.2002, pp. 702 -710

[2] – RAZAVI, B. *Design of Analog* CMOS *Integrated Circuits,* McGraw-Hill, New York, 2001.

[3] – SEDRA, ADEL S.; SMITH, KENNETH, C. Microeletrônica, 4ª edição, Makron Books, São Paulo,2000.

[4] – BADILLO, DEAN A. E KIAEI, S. "A novel low phase noise 1.8V 900MHz CMOS voltage controlled ring oscillator".