Simulation and measurements of asymmetrical delay elements: a study in temperature and supply voltage.

Martín Bremermann, Joel Gak, Alfredo Arnaud
Dep.Ingeniería Eléctrica, Universidad Católica del Uruguay
8 de Octubre 2738/DIE Montevideo Uruguay – CP.11600. *Contact email:* mbremerm@ucu.edu.uy

ABSTRACT

The time delay of a chain of asymmetrical inverters is analyzed with both measurements and simulations. Delay variations with temperature and supply voltage are investigated. Asymmetrical inverters demonstrate to be much less sensitive to supply voltage voltage, and less sensitive to temperature.

1. INTRODUCTION

Several integrated systems require the implementation of a constant time delay that does not change too much with temperature, supply voltage, or technology parameters. Untrimmed delay elements however present fluctuations, like usual R-C networks, or classic inverter chains for example. Novel topologies have been proposed in the past to overcome the problem [1,2], and the time delay of inverter chains has been investigated in detail[3]. An asymmetric inverter chain like the one in Fig.1(a), alternate small transistors sized W_{sm}, L_{sm} with very long ones sized W_{sm}, L_{long} ; $L_{long} >> L_{sm}$. The resulting delay is much different for the rising, and falling edge, of the input signal. The large delay -when long transistors have to charge/discharge large capacitors- is little sensitive to technology parameters [1]. The asymmetric inverter in Fig.1(b) incorporates a PMOS transistor connected to ground. This transistor M_D presents not only an extra capacitance to M_1, but also it opposes to M_{1a} when charging M_2 gate capacitance. The effect helps to compensate time delay variations related to supply voltage. In this paper three previously fabricated delay elements are compared:

Classical Inverter (named InvC): is a chain of 8 classic inverters with both PMOS and NMOS transistors sized W / L =4/160µm.

Asymmetrical Inverter (named InvA): is a chain of 2 inverters like in Fig.1(a) with W_{sm} =4µm, L_{sm} =2.4µm, L_{long} =480µm.

Modified inverter (named InvD): is the inverter of Fig.1(b) with W_{sm} =4µm, L_{sm} =2.4µm, L_{long} =280µm, L_D =480µm.

All the inverters incorporate input and output buffers. In the following sections, detailed time delay simulations and measurements will be presented for this three circuits while varying the temperature (-10 to 80ºC) and supply voltage (1.5 to 5V).

2. SIMULATIONS AND MEASUREMENTS

The integrated circuit was fabricated in a standard 0,8um CMOS technology. The work was divided into two stages.

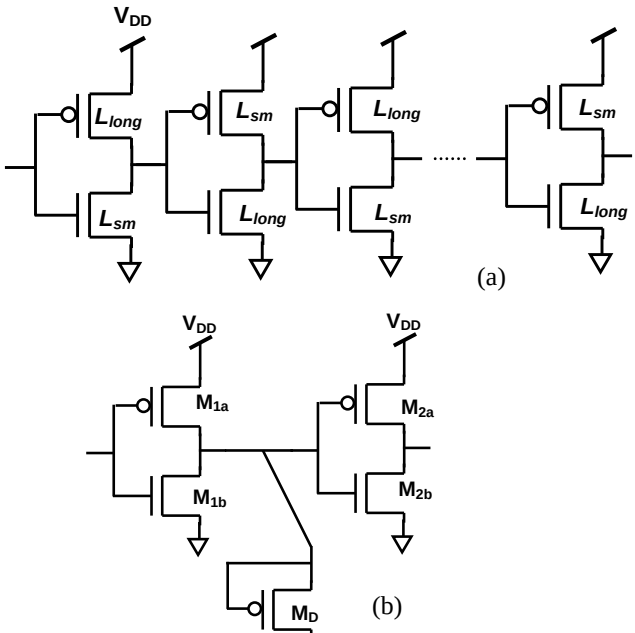

Fig 1. (a) InvA: Asymmetric inverter chain (b) InvD: Modified asymmetrical inverter chain.

In the first stage we varied the voltage supply between 0.9V and 5.0V in steps of 0.1±10mV. The procedure that we follow to test it was as follows: first we generated a 1kHz square wave with a WAVETEK FG2C function generator (into 50Ω load). Note that the main thing to bear in mind was that te supplied voltage had to be the same as the amplitude of the square wave. We used a digital oscilloscope (Tektronix TDS1002) to measure the delay t_d of the outcoming signal from the IC of each of the inversors. This procedure was repeated for each voltage. To reduce some glitches at the transistion time we used a tantalum capacitor between V_{DD} and V_{SS}. The results of this stage is shown in Fig. 2(a).

In stage two we varied not only the voltage but the temperature as well. In this case the voltage at which the IC was tested was: 1.5V, 3.0V, 4.0V and 5.0V for each temperature. The range of temperatures went from –10°C to 80°C in 10º steps. In this stage we used the same measurement techniques as we did in stage one however now the circuit was put into an oven which is used for investigation purpouses only and its tested range goes from

–100°C to 120°C. To measure the oven´s temperature it was used a digital thermometer (VOLTCRAFT 502). It has a thermocouple type K and its temperature range goes from

-200°C±0.1°C up to 1370°C. The mesurements were made at 1KHz. The results of this stage is shown in Fig. 2(b).

The program we used to simulate was SMASH 5.2.2. The simulation model was Bsim 3V3 for standard CMOS 0.8µm technology, typicall model.

3. CONCLUSIONS

The asymmetrical inverter chains behave better than classic one, because are less sensitivo to changes on the supply voltage. The modified one InvD also shows a point with a null derivative respect to V_{DD}. The three inverters show a similar behaviour with temperature, however for low supply voltages asymmetrical inverters show a negligible delay variation from -10 to 80ºC. Asymmetrical inverters enable to build more stable circuits under any of the given circunstances.

4. ACKNOWLEDGMENTS

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5. REFERENCES

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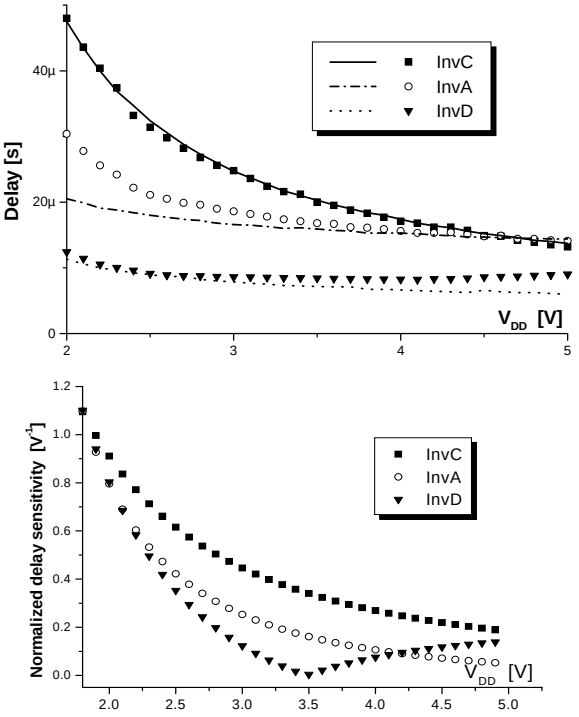

Fig 2. (a) Measured (scatter), and simulated (line) time delay t_d against supply voltage at room temp.

(b) Normalized sensitivity $NS = \frac{\partial t_d}{t_d \partial V_{DD}}$

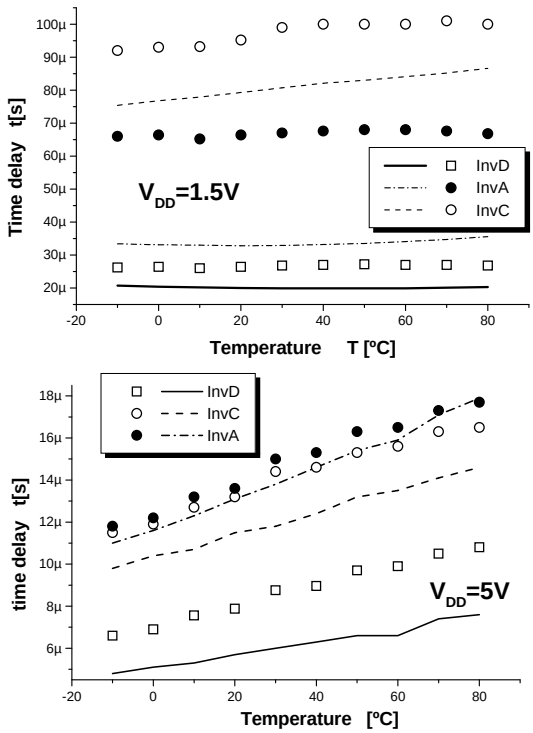

Fig 3. Time delay against temperature for InvA, InvC,InvD, at V_{DD}=1.5V(up) and V_{DD}=5V (bottom).