1Kbit x8 SRAM in 0.5µm CMOS Technology

Emilena Specht
emilenas@inf.ufrgs.br

Daniel Barcelos
danielb@inf.ufrgs.br

Renato Ribas
rpribas@inf.ufrgs.br

Instituto de Informática - Departamento de Engenharia Elétrica - UFRGS

Abstract

A university task turned into a real chip. The challenge is to design a small SRAM, which may interact with integrated processors developed for academic research. This project is an opportunity to learn more about the electrical behavior and layout of SRAMs, still having a reward: a chip materialized by MOSIS®, a silicon manufacturer.

As this kind of memories is known for fast access time, we have to deal with short response time and limitations on area.

Estimates, critical simulations and optimized layout design were steps necessary to accomplish the task, as we present in this article. Results show that the designed SRAM takes about 9ns for reading and 10ns for writing, and the final chip area is 7.5 mm².

1. Introduction

Commercial RAM manufacturers are much better at designing RAMs than the average system designer [1]. This statement brought us motivation to develop a memory. Besides, embedded SRAM can be tuned for area x speed x power tradeoffs, depending on the specific application, and hence the need to master all design steps regarding this component.

In this work, we show the design of a 1Kbit x8 asynchronous SRAM, conceived using 0.5µm CMOS technology from AMI. Magic CAD[2] and Spice tools[3,4] have been used. Our goal is to determine the optimal transistor dimensions to increase performance and guarantee correct memory operation. We also approach other memory concepts, structure, results and conclusions at last.

2. SRAM Structure

SRAM is an acronym for *Static Random Access Memory*. The term 'static' is derived from the fact that it does not need to be refreshed like a dynamic RAM. This behavior is achieved because bit cells, which hold memory values, are composed by NOT gates directly linked to each other. The amount of bit cells composes the sea of bits. Bytes in memory are placed in a sea of bits as matrix positions, addressed by lines and columns. The SRAM in question has 32 lines and 4 columns, in order to have a square chip. Other structures that take part in the memory are shown below, with a bit cell in detail.

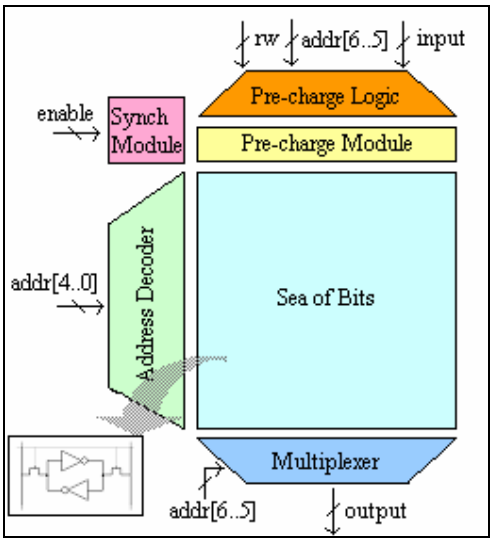

Figure 1. Memory and bit cell structure

The memory communicates with the external world through 40 pins, including 8 bits for data in, 8 for output, 7 for address, one read/write bit and the chip enable signal.

3. Read and Write Operation

The voltage values at the bit cell inverters extremes represent the value held by that bit and its respective opposite. Also, in the bit cell there are control NMOS transistors (Nc1 and Nc2 in figure 2), responsible to connect these extremes to vertical bit lines that act as capacitors. Transistors allow communication depending on the address given to the memory. The address lines are the same in a column of bits.

When there is no action in memory, all vertical bit lines are in high impedance and all control NMOS transistors are not conducting.

To set a value of a bit, one line must be charged and the other discharged, according to the value that is going to be written. Nc1 and Nc2 allow connection of lines with the bit cell. If the value to be written is the same of the current one, nothing happens. If the value is the opposite, due to transistor MOS proprieties, a 5V potential difference appears, dividing charge between P1 and Nc1, as shown in figure 2. As NMOS transistors are in fact more conductive than PMOS with the same dimensions, the voltage in the bit cell extreme drops, forcing a value change.

To read a bit value, both lines (S and notS) are pre-charged and, after that, led to high impedance. Nc1 and Nc2 establish connection, which divides charge between N1 and Nc1, as shown in figure 2 as well. Then, one line is discharged; it can be the line read or the other one, depending on the bit value. This division can be considered linear in relation with the W (width) of the NMOS transistors, and we must assure that the state of the NOT gates will not be changed at any time. Now the most critical point appears: choose the best W for N1 and N2, in order to avoid losing the bit value. To avoid this situation, the voltage in the bit cell extreme must not be higher than the NMOS threshold and the Nc1 and Nc2 width has to be significantly greater than the N1 and N2 width.

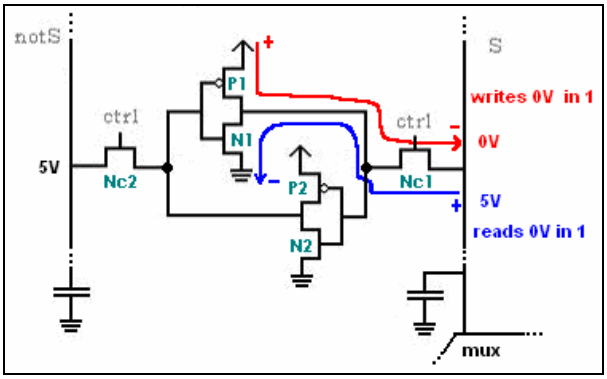

Figure 2. Bit cell reads and writes

4. Addressing and Pre-charge Control

In a way to determine the line to be accessed, each bit line control of a pass transistor is activated by a decoder: a NAND6 gate followed by an inverting buffer, which considers the 5 less significant bits of the address. It is a critical module in timing, due to the unavoidable buffer delay and line capacitance.

The byte column is activated together with pre-charge logic. Pre-charge is done by activating large transistors, a PMOS linked to Vcc (in case of charge) and NMOS linked to ground (discharge). The signals directly depend on rw input, data input value (in writing) and an internal synchronization signal conceived from an external enable input. A synchronization module is responsible for generating an internal synch signal and another input to decoder, which activates the control NMOS transistors. The synch module consists basically on a NAND gate with inputs originated from the same signal (enable), but dephased from each other to generate pulses. Instead of using internal signals, the memory may take them from external pins in case the synchronization fails.

Output data (in reading) is multiplexed according to the 2 most significant bits of the address. Since no sense amplifier is used, the column mux is also responsible to increase the noise margin of the output.

5. Results

We found the bit cell optimal width dimensions as 1.2µm for PMOS and 1.8µm for NMOS at bit cell inverters, and 1.5µm for control NMOS transistors. Memory delays are about 9ns while reading and 10ns in writing process. Decoder delay is near to 20% of total. Chip area is about 7.5mm^2. Figure 3 shows the percentage of total area occupied by each module.

Chip design has been sent to MOSIS for fabrication.

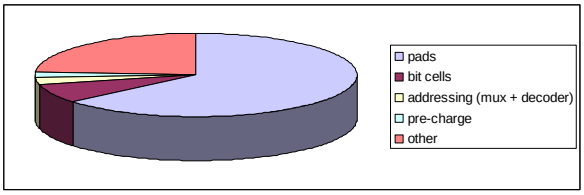

Figure 3. Memory occupation

6. Conclusions and Future work

As we expected, the SRAM design brought us a lot of knowledge, which may help in a future development of other dedicated memories, with different responses on time and area occupation.

When the chip arrives, we are going to execute test plans, using extra pins that have been connected to dedicated test points.

References

[1] Weste, N. at al. *Principles of CMOS VLSI Design.* Addison-Wesley Publishing Company, 1993, p. 566.

[2] Mayo, R. N. DECWRL/Livermore Magic Release. Western Research Laboratory. California USA, 1990.

[3] Buermen, A. et al. Spice OPUS. CADC Group, 2002.

[4] OrCAD PSpice v. 9.0 © OrCAD Inc., 1998.