A Waveform Characterization Study

Cecília Maggioni Mezzomo, Marcos F. L. Ledur, Renan Fonseca, Cristiano Santos,
Gustavo R. Wilke, Ricardo Reis
{cmmezzomo, mflledur, rafonseca, clsantos, wilke, reis}@inf.ufrgs.br

Universidade Federal do Rio Grande do Sul
Instituto de Informática - Porto Alegre /RS – Brasil

Abstract

This paper presents and study on how to represent the waveforms in a digital circuit using piece-wise linear (PWL) curves. This work targets to characterize the range of linear functions used in the PWL representation. Therefore it is possible to generate a library of lines that would be used to represent signals inside a digital circuit and compute delays. The experiments made suggest that it is not necessary to generate a library containing all possible sorts of lines, since some events are highly unprobable.

1. Introduction

Piece-wise linear (PWL) representation relies on representing a curve by small line segments. PWL representation is accurate and easy to derive when representing highly linear waveforms. In this case, few segments are needed to describe it. On the other hand, generating a PWL for non linear waveforms is not so straightforward. To achieve a good accuracy several segments are needed and the representation still contains some error. The maximum error introduced by the PWL representation must be estimated in this case.

PWL representation is widely used for modeling the electrical behavior of components and to characterize analog devices [1][2].

There are two distinct approaches to represent a waveform in a PWL fashion. In the first one the lines are homogeneously distributed over the time, regardless the linearity of the represented signal. The second strategy relies on using smaller segments of lines when the represented waveform in non linear and fewer when the waveform is more linear. It is clear that the second approach will probably produce a PWL representation with a smaller error and fewer segments. Although a better representation is achieved when the lines have distinct periods in this work the first approach will be used for the reasons discussed in section 2.

This work targets to characterize segments of lines used to represent realistic waveforms in a PWL fashion. Experiments were made to find how the slope of a linear segment changes according to the represented waveform. In section 4 conclusions are derived from the experimental results.

2. Overall Picture

The result here obtained will be used to generate a database for a switch level [3] event-based simulator. Internal signals will be represented only as PWL curves. For each linear segment within the PWL representation the correspondent segment in the output will be computed according the interpolation of values from spice simulations. This procedure is shown in Figure 1.
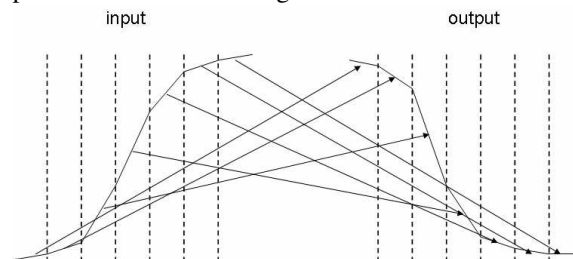

Figure 1 - Transfer function scheme

To reduce the number of simulations and the database size but still accurately compute the output waveform it is necessary to study the behavior of PWL functions. Considering the constraints of a digital design and the constraint imposed by the technology it is reasonable to expect that within a fixed period there is a maximum excursion for the voltage. By knowing how much can this variation be it is possible to simulate and store in the database only values close to the one that will be observed in practice.

3. Experiments

The experiments were conducted using a 0.13 microns technology.

A circuit composed by a chain of six inverters was simulated to observe the behavior of a PWL representation for a realistic signal. A voltage step was applied in the input of the first inverter. The

signal was sampled in the output of the fourth inverter. Figure 2 illustrates the simulated circuit.
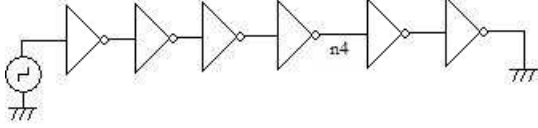

Figure 2 - Inverter chain

To simulate different load situations the size of the inverters 4 and 5 were independently multiplied by a factor of 1, 2, 4, 8 and 16. Figure 3 shows how the waveform is affected when the ratio between the fourth and the fifth inverter is changed from 16 to 1/16.
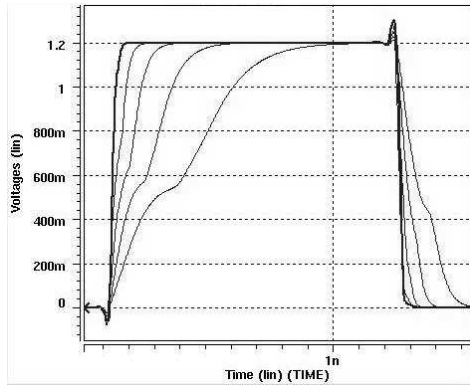

Figure 3 - Load effect on waveform

The study consist on describing the waveform in the output of inverter 4 as a PWL signal evaluating its error and characteristics. Three different sample intervals are used in the PWL representation, 5ps, 10ps and 20ps.

4. Results

Due to non linearity in the sampled waveform, PWL representation introduces an error in the representation. Figure 4 shows a situation where the PWL representation can be very inaccurate in relation to the real signal. Table 1 reports the maximum error observed for each experiment when a sample interval of 20ps was used.
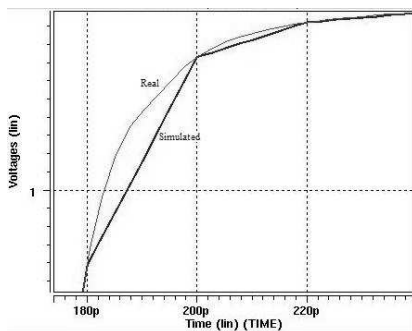

Figure 4 - Error in PWL representation

M4	M5	Max Error
1	1	5,53%
1	2	5,48%
1	4	3,80%
1	8	2,04%
1	16	1,02%
2	1	2,05%
4	1	3,08%
8	1	5.68%
16	1	3.42%

Table 1 - Maximum error

The slope of the linear segments used to compose the PWL representation were measured. The results were grouped according to voltage from were the linear segment begins. The obtained results can be seen in Table 2.

	0,24 V	0,48 V	0,72 V	0,96 V	1,2 V
Vmin	-0,152	-0,214	-0,424	-0,726	-1,05
Vmax	0,845	0,23	0,423	0,229	0,158

Table 2 - Slope variation according to valtage intervals

4. Conclusions and Future Works

Our results clearly show that the PWL representation can be used to represent signals with small errors. It is also important to mention that by observing the behavior of real signals it is possible conclude that the linear segments are bounded by technology and electrical constraints and therefore can not be too steep. When creating a library of linear segments as mentioned in section 2 the number of values can be drastically reduced once several situations may never occur.

It would be interesting to evaluated other strategies to represent the waveform such as using a variable step to sample the signal according to the non linearity of the waveform or using a voltage step instead of a time step.

5. References

[1] A. Dharchoudhury, S. M. Kang, H. Cha, and J. H. Patel. Fast Timing Simulation of Transient Faults in Digital Circuits. Proc. of IEEE Int. Conf. On Computer Aided Design, pages 719 – 726, 1994.

[2] Martinez, J.A., Kurzweg, T.P., Levitan, S.P., et. al. System Level Simulation of Mixed-signal Multi-domain Microsystems with Piecewise Linear Behavioral Models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. February 2003, Vol. 22, Pg 139-154.

[3] J.K. Ousterhout. Switch-Level Delay Models for Digital MOS VLSI.Proc. of the 21st Design Automation Conference, 1984.