DOPPLER ULTRASOUND SIGNAL PROCESSING BASED ON AN FPGA

I. G. Vazzoler, B.S.Dupczak, J.F.R. Baggio, R. Moraes
Instituto de Engenharia Biomédica, Universidade Federal de Santa Catarina, Florianópolis, SC, Brazil

Abstract–**This work describes an implementation in a Field-Programmable Gate Array (FPGA) to process quadrature ultrasound Doppler signals in real time. The FPGA controls an A to D converter to sample the Doppler signals and applies complex FFT to consecutive 10.7 ms signal intervals. The results are transmitted to a computer via USB. The computer runs software that presents the sonogram on the screen in real time. An example of sonogram obtained with the developed system is presented.**

Keywords –**Ultrasound, blood flow, sonogram, FPGA.**

I. INTRODUCTION

Dialysis access failure remains the major cause of morbidity among patients undergoing hemodialysis. The National Kidney Foundation guidelines for vascular access recommend access surveillance to improve patient care [1].

Reduced blood flow reveals access malfunction. Methods to detect access failure based on continuous wave (CW) Doppler systems are being proposed to implement surveillance programs at lower cost [2,3].

The probe of directional CW Doppler systems contains two transducers, a source and a receiver. The first emits the ultrasound waves into the tissues and the second receives the backscattered signal from the red cells. The received signal, after converted to an electrical one, is demodulated by the Doppler system, yielding quadrature Doppler signals for further processing. As the blood flow profile changes during the cardiac cycle, the quadrature Doppler signals have their frequency content modified [4].

To display the distribution of the flow velocity profile in a vessel, complex FFT (CFFT) is applied to the quadrature Doppler signals to separate their components into frequency ranges of equal bandwidth. For each frequency range, the intensity is calculated. This intensity represents the amount of blood flowing at a certain speed. The presentation of the Doppler spectrum at consecutive time intervals is called a sonogram. The spectra are shown on axes of time and frequency, with the relative intensities of the frequency components displayed in a color-coded mode [4].

Most commercial and research systems employ commercial DSP boards to apply CFFT to the Doppler signals [5]. It was recently shown that it is possible to process the Doppler signals using personal microcomputers [6].

To further reduce the costs of CW Doppler systems, this work proposes the use of FPGA to process the Doppler signal. This approach allows the use of less powerful computers, such as handheld ones, to present the sonogram. In addition, the system becomes more portable, and therefore, more suitable for clinical application.

This work describes the implementation of Doppler signal processing on a FPGA, aiming cost reduction and portability of CW Doppler systems.

II. METHODOLOGY

Figure 1 shows the block diagram of the proposed system.

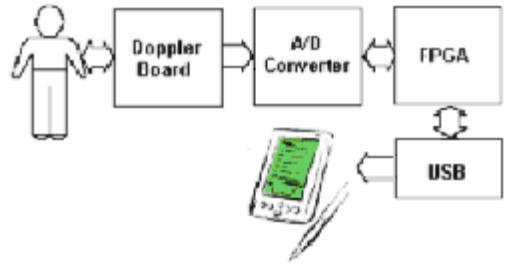

Fig. 1. Block diagram of the developed system

The Doppler board developed is described elsewhere [7]. The parts used in the developed system are: the Spartan-IIE FPGA (Xilinx), the A to D converter ADS7864 (Burr-Brown) and the USB interface FT245BM (Future Technology).

Figure 2 presents a schematic diagram of the functions implemented in VHDL and executed by the FPGA. The quadrature Doppler signals are simultaneously sampled at the rate of 24kHz by the ADS7864. Two words of 12 bits are generated.

A state machine controls the ADS7864. The acquired samples are stored into two sets of dual port 512 word (12 bits) buffers. After the acquisition of the first 512 samples, the second set begins to be fulfilled while the first set is read. At the completion of the second set, the state machine begins to store the new samples into the first set in a circular mode. Each set of buffers holds 256 pairs of samples of the in-phase and quadrature Doppler signals.

After sampling 256 pairs of data, the samples are sent to the core that calculates the CFFT [8] and to the computer. The quadrature Doppler signals sent to the computer can be reproduced by speakers (or headphone) in order to help the operator to place the probe on the vessel.

The CFFT results are copied to other two buffers from where they are sent to the computer via USB at the rate of 144 kbps. Another state machine transfers the CFFT results from the FPGA buffers to the FT245BM. A program written in C++ presents the sonogram on the computer screen.

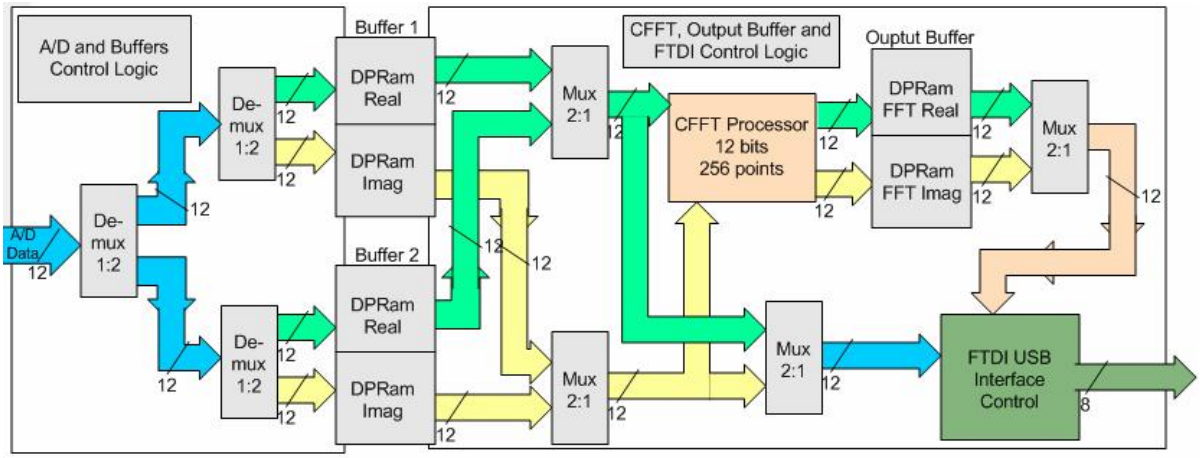

Fig. 2. Block diagram of the tasks performed by the FPGA to control the acquisition and processing of Doppler signals. The FPGA also controls an USB interface CI to send the CFFT results to a computer. The arrows stand for the data flow within the FPGA.

III. Results

The implemented project occupies 979 slices of the Spartan-IIE FPGA (41 % of the total capacity), 4 kbytes of RAM (57% of the total capacity), running at a maximum frequency of 78.2 MHz.

The total acquisition time for 256 pairs of Doppler samples is 10.67 ms. The CFFT is calculated in 25.8 µs. Figure 3 depicts an example of sonogram generated by the implemented system.

Fig. 3. Example of sonogram obtained with the developed system for Doppler signals sampled at a vascular access.

IV. Discussion and Conclusion

The obtained results show the feasibility of using FPGA to process Doppler signals. Dedicated hardware based on a DSP processor could also carry out the Doppler signal processing in real time. Nevertheless, the implementation in FPGA, using VHDL, presents advantages. An FPGA project can be promptly compiled to new ICs of different manufacturers. To port a DSP processor implementation to a newer device, code changes would be required due to the different addresses of the memory, interrupt vectors and peripherals. Besides, more than one instance of the project can be programmed into a FPGA to implement a multi-channel Doppler system. Such implementation would allow more than one vessel to be simultaneously interrogated to gain a better insight of the blood circulation.

It is also possible to implement control circuits of the Doppler board into the FPGA to reduce the costs of the whole system without decreasing its real time performance. For instance, the FPGA can generate the quadrature signals to demodulate the Doppler signals and control the gain of amplifiers.

V. References

[1] National Kidney Foundation. "Clinical Practice Guidelines for Vascular Access". *Am. J. Kidney Dis.*, 37 (Suppl. 1): S137.81, 2001.

[2] M. Paun, K. Beach, S. Ahmad, R. Hickman, M. Meissner, C. Plett, E. Strandness. "New ultrasound approaches to dialysis access monitoring", *Am. J. Kidney Dis.*, no. 35, pp. 477-481, 2000.

[3] P. S. C. Molina, R. Moraes, J. F.R. Baggio, E. A. Tognon. "Continuous wave Doppler methods to dialysis access monitoring", *26th Annual International Conference of the IEEE EMBS*, pp. 2341-2344, San Francisco, CA, USA, 2004.

[4] D. H. Evans, W. N. McDicken. *Doppler Ultrasound: Physics, Instrumental, and Clinical Applications*, John Wiley & Sons Inc, 1990.

[5] N. Aydin, *Computerised graft monitoring*, Leicester-UK, Thesis (Doctor of Philosophy), Division of Medical Physics, Faculty of Medicine, University of Leicester, 1994.

[6] J.F.R. Baggio, P. S. C. Molina, R. Moraes. "Software para processamento de sinais Doppler em tempo-real em IBM-PC", *III Congresso Latino Americano de Engenharia Biomédica*, João Pessoa, PB, BR, 2004.

[7] P. S. C. Molina, R. Moraes, J. F.R. Baggio, E. A. Tognon, "System for Vascular Dialysis Access Surveillance", *26th Annual International Conference of the IEEE EMBS*, pp. 2352-2355, San Francisco, CA, USA, 2004.

[8] M. Zhao, "Radix 4 Complex FFT", http:// www.opencores.org, 2003.