

Study of Application of Inductive Source Degeneration in LNA

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Abstract - The Low-Noise Amplifier (LNA) is an essential block for wireless systems and it is responsible for the input weak signal amplification of receivers. In this work the main architectures of LNA are presented and its specifications are discussed. Additionally, the common-source architecture with degeneration of source is analyzed and one is designed in a 0.35 μ m CMOS technology. Simulation results show that the designed circuit presents a 48.8 Ω input impedance and 12.3 dB gain, with power supply of 3.3 V and power consumption of 28.5 mW.

I. INTRODUCTION

The advantages of portable communication products and wireless systems such as mobility and versatility are the reasons for the high increase of wireless systems telecommunication market has been expended and consequently motivates researches in the area to reach better performance and lower costs [1].

The weak signal received at the antenna of a reception wireless system requires a first amplification to detect it adequately to apply the necessary process. The LNA (Fig. 1) is a block that must perform this function where the gain and noise are the most important features.

The LNA design is critical because it must supply an enough gain to low power levels that arrive from antenna without degrading the signal-noise ratio (SNR) and it must supply stronger signals with low distortions and low power consumption. As the first stage of a receiver is the antenna, there is the necessity of a specific input impedance of 50 Ω to accomplish a maximum power transfer. Because of this, the LNA requires a compromise between gain, low noise figure, high linearity, input/output matching and low power consumption [1,2].

II. LOW NOISE AMPLIFIER – LNA

The LNA is a block that can be utilized by several front-end circuits like receivers and transceivers, each LNA design with its own specifications. At Literature, three different strategies

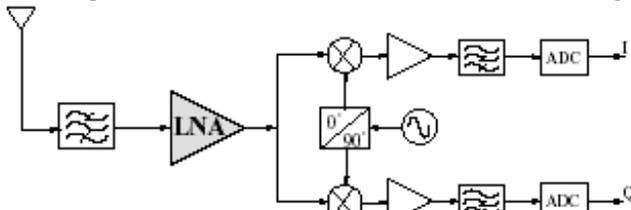


Figure 1: Diagram of a homodyne receiver.

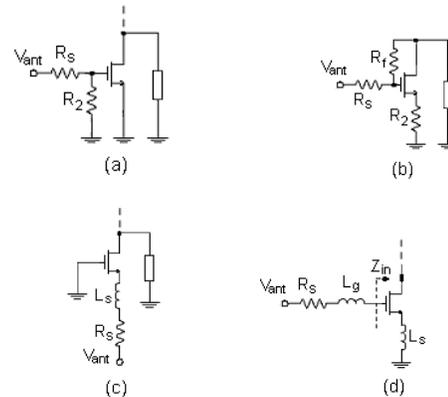


Figure 2: Common-source with resistive coupling (a); Common-source with feedback (b); Common-gate (c); Common-source with inductive source degeneration (d).

can be found for LNA in the CMOS design, impedance matching to reach maximum power transfer and minimum noise factor and strategy of design for high linearity [3,4]. Because of different conditions of design, several architectures are proposed and the most utilized is depicted at the Fig. 2. This architecture tries to establish better gain, input matching and noise figure.

III. INDUCTIVE SOURCE DEGENERATION

An architecture chosen for this work is the circuit of Fig. 2(d), which presents a common-source LNA amplifier with inductive source degeneration. In this design we worked with the limit of technology utilizing 0.35 μ m NMOS transistor model of AMS manufacture process. The main point of this work is to analyze the voltage gain obtained from passive elements at the input amplifier circuit. Fig. 3 presents the AC model of the simplified LNA.

Through the resonant effect viewed at the input, the impedance z_{in} is obtained by only a resistive effect (3).

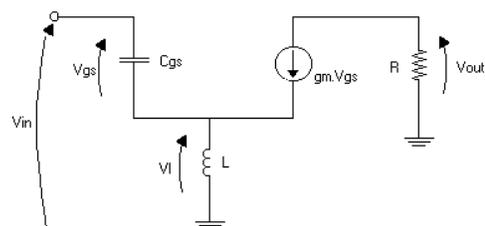


Figure 3: Analysis of low signals at a LNA with inductive degeneration.

$$v_{in} = v_{gs} + v_l \quad (1)$$

$$v_{in} = i_{in} \cdot x_C + i_{in} \cdot \left(g_m \cdot \frac{L_s}{C_{gs}} + x_l \right) \quad (2)$$

$$R \cong g_m \cdot \frac{L_s}{C_{gs}} \quad (3)$$

At resonance, the input current reaches the maximum value and consequently maximum voltage value at the capacitor is reached.

$$|v_{gs, \max}| = \frac{1}{\omega \cdot C_{gs}} \cdot \frac{v_{in}}{R} \quad (4)$$

$$\left| \frac{v_{gs}}{v_{in}} \right| = \frac{1}{2\pi \cdot f \cdot g_m \cdot L_s} \quad (5)$$

The circuit allow the design $(2\pi \cdot f \cdot g_m \cdot L) < 1$ and obtains a voltage gain at (5), contributing with total LNA voltage gain (6).

$$A_V = \frac{-g_m \cdot R_{out}}{s \cdot C_{gs} \cdot z_{in}} \quad (6)$$

An inductor L_g was added between v_{in} and the transistor gate (Fig.2d) additionally to obtain more control of voltage gain, because L_s is fixed to adjust z_{in} , it is represented by following expression.

$$z_{in} = R_g + R_s + \frac{g_m \cdot L_s}{C_{gs}} + j\omega \cdot \left((L_g + L_s) - \frac{1}{\omega^2 \cdot C_{gs}} \cdot (1 + g_m \cdot R_s) \right) \quad (7)$$

where R_g and R_s are the series parasitic resistances of the inductors.

IV. SIMULATION

Fig. 4 presents the frequency response of the impedance z_{in} in the LNA simulated with electrical simulator Orcad and it shows on the operation frequency of 1.7GHz an input impedance of 48.9Ω so that to obtain a reflection coefficient S_{11} of -9.6dB. The following simulation depicted in Fig.5 presents the voltage gain A_v by frequency, where (a) is the gain of the circuit (v_{out}/v_{in}), it reached a value of 12.3dB whereas curve (b) presents the gain v_{gs}/v_{in} of 3.9dB obtained at resonance of the input amplifier circuit. Table 1 refers of values used in this topology.

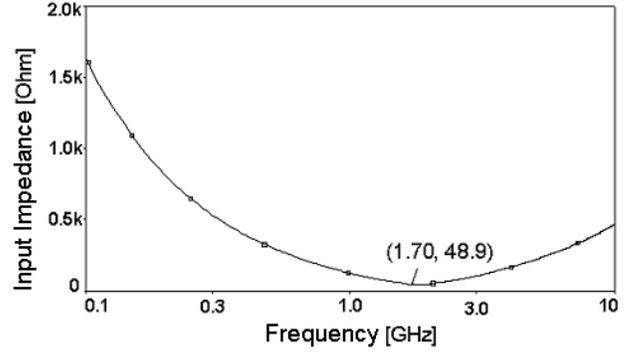


Figure 4. Simulation to obtain the input impedance.

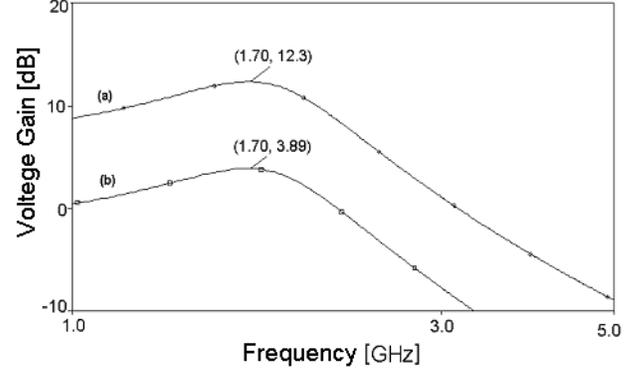


Figure 5. Simulation of the LNA voltage gain (a) and the input impedance from RLC circuit (b).

V. CONCLUSION

In this paper, the most utilized architecture of LNA could be analyzed, which highlighted the architecture that increased an inductive degeneration at the source, then it allowed a perfect input impedance coupling and an increase of voltage gain by the resonant effect obtained by a simple RLC circuit in the input of the LNA.

An voltage gain of 12.3dB could be reached with the impedance coupling at the input impedance given by S_{11} equal to -9.6dB.

REFERENCE

- [1] Y. Ge and K. Mayaram, "A Comparative Analysis of CMOS LNAs for RF Applications," in ISCAS. IEEE, 1998, pp. 349–352.
- [2] D. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS Low Noise Amplifier," IEEE J. Solid-State Circuits, vol. 32, no. 5, pp. 745–759, 1997.
- [3] B. Razavi, "CMOS Technology Characterization for Analog and RF Design," IEEE J. Solid-State Circuits, vol. 34, no. 3, pp. 268–276, 1999.
- [4] T. H. Lee, The design of CMOS Radio Frequency Integrated Circuits. Cambridge University Press, 1998.

Table 1: Parameters of the LNA.

| Parameters | C _{gs} | G _m | C _{ox} | W | L | R | L _g | L _s | R _{load} | f ₀ |
|------------|-----------------|----------------|-------------------|-----|------|---|----------------|----------------|-------------------|----------------|
| Values | 1.50 | 0.74 | 0.46 | 600 | 0.35 | 5 | 7.9 | 0.8 | 50 | 1.7 |
| Units | pF | mS | mF/m ² | μm | μm | Ω | nH | nH | Ω | GHz |