A Charge-based Transistor Model for a Switch Level Simulator

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Abstract

It is well known that switch level simulation is highly inaccurate in comparison to electrical simulation. The main source of inaccuracy is due to the fact that transistor are approximated by simple linear resistors. This paper proposes a new way of modeling the transistors in order to achieve better accuracy. A charge-based model for the transistor was derived from spice simulations. A methodology is proposed to used this model inside a switch level simulator. Results in terms of the cost to generate this model are shown.

1. Introduction

A switch level simulation approximates a transistor by a linear resistor in series with a switch [1][2]. Switch level simulator are fast but inaccurate due to that. On the other hand electrical simulators are very accurate but the execution times are very high. In this paper new model for a switch level simulator is proposed. As in a switch level simulator, each segment from a voltage source passing through one or more transistor's channel and ending in a transistor gate will be treated independently. To improve the accuracy a new model of a switching level involving not resistances, but charge variations in a small time is proposed.

2. The method

We desire to find the accumulation of the charges on the drain of a transistor. On the figure 1, a NMOS transistor is excited by two sources (V_{DS} and V_{GS}). The integral of the current Id represents the charge variation on the drain.
Even though V_{DS} is, in general, an output of the transistor, it's necessary to have a current on the drain. Besides, the variation of V_{DS} (for one V_{GS}) produces just one value of the charge variation, on a simple circuit of the figure 1. We can come to this conclusion if we imagine the rest of the network as it's Thévenin's Equivalent (ignoring the resistance).

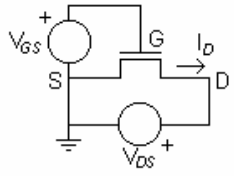

Figure 1: A NMOS Circuit with Voltage Sources

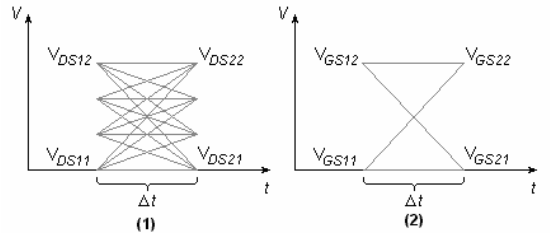

Figure 2: Varying the sources

The transistor is a non-linear component, so there isn't a way to calculate the charge variation with a simple formula. So, simulations should be made. To do that, HSpice was used.

3. An algorithm for the method

For obtaining the charges, two stages are needed. First, thirteen parameters are enough to make a good table of charges. The four first are V_{DS11}, V_{DS12}, V_{DS21} and V_{DS22}, respectively, the bottom first, the top first, the bottom second and the top second voltages of V_{DS}. Next, we have n_{VDS1}. It indicates how many voltages we want between the first voltages, V_{DS11} and V_{DS12}. Then, we have n_{VDS2}, the same way for the second voltages. The next six parameters are similar to the six first, except they're for the source V_{GS}. The last parameter is Δt, the time between the first and second voltages. The figure 3 shows an example for both sources, where $n_{VDS1} = n_{VDS2} = 4$, and $n_{VGS1} = n_{VGS2} = 2$. A table now can be built in the HSpice format. A single line of this table contains the ramp source V_{DS} (one segment of figure 2(1)) and the ramp source V_{GS} (one segment of figure 2(2)). Therefore, the table will have $n_{VDS1} \times n_{VDS2} \times n_{VGS1} \times n_{VGS2}$ lines.
After we have the sources table, HSpice can be run. The measurement command measures the charge in

D. So, another table now can be build, containing the sources and the charge variations in D.
Two charge tables where build, one for a NMOS and another for a PMOS transistor, both with a w=0.13 and l=0.6.

4. Validating the Method

In the validation phase, an inverter with the desirable transistor characteristics was used, connected to a capacitive load. On the figure 3, we have a voltage source connected to the inverter, $V_{in}(t)$, and an output voltage, $V_{out}(t)$. For the NMOS transistor, $V_{GS}(t) = V_{in}(t)$, and $V_{DS}(t) = V_{out}(t)$. And for the PMOS transistor, $V_{GS}(t) = V_{in}(t) - V_{DD}$ and $V_{DS}(t) = V_{out}(t) - V_{DD}$. The source $V_{in}(t)$ was a ramp which grows from 0 to V_{DD} in 0.1ns.

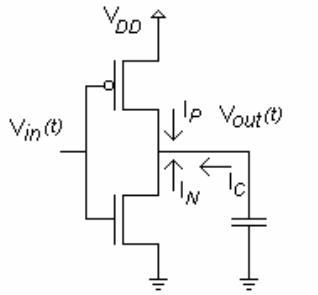

Figure 3: Inverter circuit used on validation

Interval	Error (%)
0-10ps	-0.62
10ps-20ps	0.15
20ps-30ps	0.15
30ps-40ps	0
40ps-50ps	-0.04
50ps-60ps	0.57
60ps-70ps	0.4
70ps-80ps	1.1
80ps-90ps	1.8
90ps-100ps	2.2

Table 1: Results of the simulations

After we have simulated the circuit with HSpice, we discretize $V_{in}(t)$ and $V_{out}(t)$ using intervals of 10ps. On each interval, we obtain the discrete waveforms of V_{DS} and V_{GS} for both transistors (ramps), and seek the respective charge variations (ΔQ_N and ΔQ_P) on the tables. The charge on the capacitor is obtained by the capacitor formula, $\Delta Q_C = C^*\Delta V_{out}$.
Now, according to Kirchhoff's Currents Law, the sum of the currents on the node $V_{out}(t)$ is zero. If we choose a Δt which is sufficient small, the sum of the charge variations tends to be zero. This experiment is reported in table 1.

The percentage error represents the difference between the actual charge in the output capacitor in relation to the charge computed by the proposed method.

5. An usage for the method

We can idealize a switch level simulator that, given a source connected to a logic gate, calculates the output signal. The initial conditions are known (the charges on the transistors and the charges on the output, that is, the capacitor).
First of all, the simulator choses a voltage to the output. Then, it verifies if this voltage satisfy the charge variations. Next, the simulator will pick a new value to the output based on the value computed according to the charge variation produced by the first iteration. The method goes on until the voltage chosen is the same computed according to the charge variations.
This procedure is applied for all segments composing a PWL representation of the input signal as represented in figure 4.

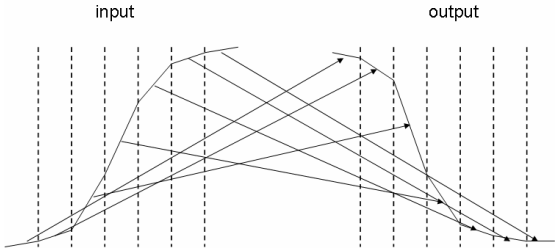

Figure 4: Finding the output waveform

6. Conclusions and Future Works

The proposed method has shown to be accurate as shown by table 1. More experiments are needed to prove that the method is valid for other gates besides the inverter. It is also needed to show that the proposed approach is faster than an electrical simulation but almost as accurate when targeting delay evaluation or power estimation.

7. References

[1] J.K. Ousterhout. Switch-Level Delay Models for Digital MOS VLSI.Proc. of the 21st Design Automation Conference, 1984.

[2] C.Y. Chu and M.A. Horowitz. Charge-Sharing Models for Switch-Level Simulation, IEEE Transactions on CAD, vol. CAD-6, No. 6, November 1987.