Elmore-based Interconnect Delay Models

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Abstract

Interconnects are playing a major role in determining the delay of today designs, being necessary to accurately generate fast estimates of interconnect delay in different level of abstractions. However being very pessimistic for nodes close to the driver, Elmore delay is the most widely used metric. This paper presents a comparative study about 3 different Elmore Delay Based methodologies. Results show that the interconnect delay estimation can be improved in relation to the traditional Elmore delay estimates without greatly increasing the execution times.

1. Introduction

With the scaling down of the physical dimensions in deep submicron (DSM) technologies, the RC interconnect delays are rising up. Interconnect delay are dominating the total delay of the circuit and so it must be taken into account in many levels of physical synthesis.

Some physical synthesis tools need a fast computation of the delay because it will be computed at every iteration of the algorithm. The exact calculation for the delay on a RC tree is not easy to compute fast enough. All the components of the circuit have an influence on the response in a manner that the calculation cannot be divided in parts to reduce the computation time.

To overcome this problem, models that approximate the delay are used. These models need to be fast to compute and also should give a good approximation of delay. In this paper, we briefly explain four of these models and then compare their accuracy using SPICE simulations as reference. The models studied are based on Elmore Delay Model and have basically the same computational cost. They are: Elmore Delay [6], Scaled Elmore Delay [3], Effective Capacitance based Model [2] and Fitted Elmore Delay [1].

2. Interconnect Delay Models

2.1 Elmore Delay (ED)

The idea behind Elmore is to analyze the impulse response *v'(t)* of a circuit, which is the derivate of the step response *v(t)* [4]. Then we observe the impulse response, such as in figure 1, as a distribution function. So, the 50% point delay of a monotonic step response is the median (τ) of this function.

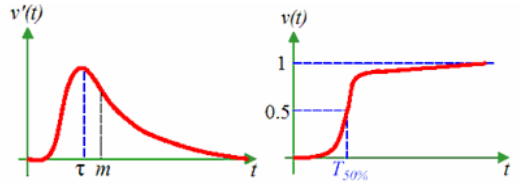

Figure 1 – Analysis of impulse and step response.

Since obtaining the median of a function is not an easy job, Elmore approximates the median by the mean *(m)* of the function *v'(t)*. The mean is calculated indirectly by the first moment of the impulse response, where comes from the following formula:

$$ED_i = \sum R_n C_n \qquad (1)$$

The sum is over every node *n* on the path between the source and node *i*. R_n is the resistance of the node *n*; C_n is the total capacitance downstream the node *n* [6].

2.2 Scaled Elmore Delay (SED)

This model is basically the same as ED, but it is scaled by a factor in order to get more accurate results. The major result is that the interconnect delay will have a different weight in the total delay if SED is used instead of ED.

If we calculate the delay for a simple RC circuit, we will find out that the exact delay is equal to *ln(2)**R*C. ED for the same circuit is R*C. SED makes a generalization of this fact and concludes with the following formula:

$$SED_i = 0.69 ED_i \qquad (2)$$

2.3 Effective Capacitance Model (ECM)

The ECM model tries to deal with an effect that has become more evident in the newest technologies

due to the rising up of interconnect resistance. The effect of resistive shielding is clearly not captured by Elmore, and we can note it just looking at the formula (1).

The solution given by ECM is to compute an effective capacitance for each node and use it instead of the sum of all capacitances downstream the node. Effective capacitance is calculated in two steps.

First a π-model is calculated for each node of the tree representing the net downstream the node [5]. After, the π-model is converted to the effective capacitance [2]. This conversion can be made to satisfy just one moment in the time. This moment is the delay we are searching for. So, an initial estimative of the delay is necessary, which is the ED itself.

2.4 Fitted Elmore Delay (FED)

FED model is an attempt to adjust ED by adding coefficients to terms of ED formula in order to get results closer to the results given by SPICE simulations. ED formula is separated in the following six terms:

*driver resistance * wire capacitance*
*driver resistance * wire fringing capacitance*
*driver resistance * load capacitance*
*wire resistance * wire capacitance*
*wire resistance * wire fringing capacitance*
*wire resistance * load capacitance*

So there are six coefficients which are determined through multiple linear regression with the data generated by simulations.

The values of the components are different for each simulation and the delay must be measured in every simulation.

3. Experimental Results

A tool was implemented to compare ED, SED, ECM and FED metrics with results obtained from SPICE simulations. This tool receives a description of an RC tree in spice-like netlist as input and returns a list of delays for each node in the RC tree, considering the different metrics.

Two different topologies are analyzed by the tool in order to provide an insight about the models. In table 1 there are the results for a random tree with 24 nodes, and in table 2, the results for a single wire. The results are normalized to Spice simulations. For FED the leaf nodes were considered load capacitances.

Table 1 – Delay comparison for a 24 nodes RC tree.

Node	ED	SED	ECM	FED
n1	3,48	2,41	2,79	2,55
n10	1,83	1,27	1,55	1,33
n12	1,56	1,08	1,37	1,14
n15	1,47	1,02	1,30	1,08
n17	1,36	0,94	1,22	0,99
n18	1,33	0,92	1,18	0,98
n22	1,28	0,89	1,16	0,94

Table 2 – Delay comparison for a 20 segments RC line.

Node	ED	SED	ECM	FED
n1	17,54	12,11	5,87	13,31
n5	3,28	2,28	1,75	2,48
n10	1,60	1,11	1,11	1,21
n15	1,36	0,94	1,02	1,03
n20	1,31	0,91	1,02	0,99

The ED and ECM models present positive error (upperbound) for all nodes in these test cases. The relative inaccuracy of ED in different nodes of the circuit is not affected by the SED factor. As expected, FED presented results similar to SED, and for some nodes they show a sub estimative, what is not acceptable for worst case timing analysis purposes. The ECM model has done well in these test cases: it did not underestimate the delay and presented a reasonable accuracy when compared to SPICE simulations.

4. Conclusions and Future Works

In this paper we have evaluated 4 models that can be used to estimate the delay on a RC tree. None of them presented tighter results for timing analysis, since their primary attribute is to be fast to compute. There are models which provide better accuracy, but are computationally expensive. The search for a model that combines these two characteristics is a work to be done.

5. References

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