Fabrication and Electrical Characterization of MOS Capacitors – Chemical Cleaning Evaluation

Rodrigo de Jesus Marques[1,2] and Victor Sonnenberg[1,2]
[1]Faculdade de Tecnologia de São Paulo - FATEC/SP/CEETEPS – Brazil
[2]Laboratório de Sistemas Integráveis da Universidade de São Paulo
e-mail: rodmar@lsi.usp.br and sonnen@fatecsp.br

Abstract: The goal of this work is to present the results of the electrical characterization of Metal-Oxide-Semiconductor (MOS) capacitors fabricated by varying cleaning processes, which purpose was to reduce the effective oxide charge density. Wafers with gate oxides grown for 50 min and 25 min were compared. The thinnest oxide was 10 nm thick. Parameters that were extracted from Capacitance-Voltage and Current-Voltage curves are presented.

1. INTRODUCTION

Currently, a great diversity of cleaning types exists aiming at removing impurities from the surface of silicon wafers. The most common impurities are metals, metallic compounds and organic particles. These impurities, especially in critical processes as the gate oxidation, influence directly in the performance and the MOS transistor characteristics, in ULSI (Ultra-Large Scale Integration) circuits [1,2].

To understand the physical and chemical mechanisms of impurity removal is important for evaluating the cleaning process.

Due to this fact, the electrical characterization of the gate oxide is very important [2,3].

2. EXPERIMENTAL PROCEDURES

MOS capacitors were fabricated on (100) p-type substrate with acceptors concentration of 2.5×10^{15} cm^{-3} and resistivity of 10~20 Ω.cm in three wafers with different conditions. The wafers were submitted to the following processes sequence:

A. Chemical Cleaning

The wafer 1 (sample 1) was submitted to the extended RCA [3] cleaning process, as following:

- 4 H_2SO_4 + 1 H_2O_2 (10 minutes, 115°C);
- 4 H_2O + 1 H_2O_2 + 1 NH_4OH (13 minutes, 80°C);
- 4 H_2O + 1 H_2O_2 + 1 HCl (13 minutes, 80°C) and
- 20 H_2O + 1 HF (100 seconds, ambient temperature).

DI water rinsing was carried out after each cleaning step for 5 minutes.

The samples 2 and 3, were submitted to a second type of cleaning, that was basically the standard one, with some variations:

- In the second stage, the volume of NH_4OH was reduced to 0.25, and in the third stage, the H_2O_2 was removed.

B. Thermal Oxidation

Two oxidation processes were performed. Both processes were realized at 900ºC, but for 50 minutes in samples 1 and 2 and for 25 minutes in sample 3.

C. Polysilicon Deposition and Doping

Intrinsic polysilicon film of 300 nm was deposited by LPCVD (Low Pressure Chemical Vapor Deposition) process, followed by a doping process by PSOG (Phosphorous Spin On Glass), in N_2 ambient for 50 minutes at 1050 °C in all samples.

D. Aluminium Metalization

Aluminium films of 500 nm were deposited by thermal evaporation at the front and backsides of the samples, for making electrical contact to the devices.

E. Lithography

By lithography process, capacitors with area of 9×10^{-4} cm^2 were defined.

F. Sintering Process

All samples were cut into two halves and one half of each sample was submitted to the sintering process, that was realized for 30 minutes in ambient of forming gas at 430 °C. The sintered half wafer were named S and the other one with NS.

3. EXPERIMENTAL MEASUREMENT RESULTS

The oxide thickness (t_{ox}) was obtained from physical (elipsometer) and electrical (C-V curves) measurements and similar results were obtained.

3.1.Capacitance-Voltage (C-V) Curves

The high frequency capacitance-voltage (C-V) curves from the capacitors were measured by LCR meter HP4280 at 1 MHz. These curves are presented in Figure 1.

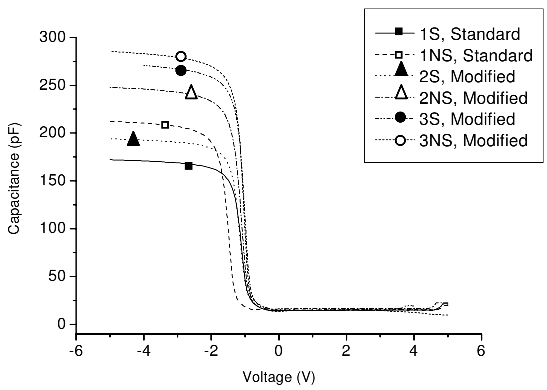

Figure 1: C-V curves from MOS capacitors for all analyzed samples.

The t_{ox}, oxide charge density (Qss/q), flat band voltage (V_{fb}) and threshold voltage (V_t) parameters values were obtained from high-frequency C-V curves [4]. The average values are summarized in Table 1.

Table 1: Average extracted parameters from high-frequency C-V curves

Sample	Cleaning	t_{ox} (nm)	Qss/q ($\times E11$ cm^{-2})	V_{FB} (V)	V_t (V)
1S	Standard	17.55	2.58	-1.08	-0.13
1NS	Standard	14.00	6.49	-1.24	-0.15
2S	Modified.	15.80	3.37	-1.04	-0.12
2NS	Modified	12.20	3.70	-1.14	-0.14
3S	Modified	10.50	2.40	-0.92	-0.17
3NS	Modified	9.92	2.56	-0.97	-0.18

The V_{fb} values of the capacitors have a variation depending on the sintering process. This process allows reducing the interface charges and dangling bonds, thus causing a charge reduction after the sintering as observed in all sintered samples.

The difference between the oxide thicknesses on the samples causes a variation in maximum capacitance. As can be observed in Figure 1, the maximum capacitance for not sintered (NS) is higher than in sintered (S) samples.

3.2 Current-Voltage (I-V) Curves

The current-voltage (I-V) curves were measured by picoamperimeter HP4140. Some of the obtained I-V curves are shown in Figure 2, for all analyzed samples. By these curves, the breakdown voltages (V_{BD}) were obtained at the point where the current increases strongly and the oxide is ruptured, as shown in Figure 2.

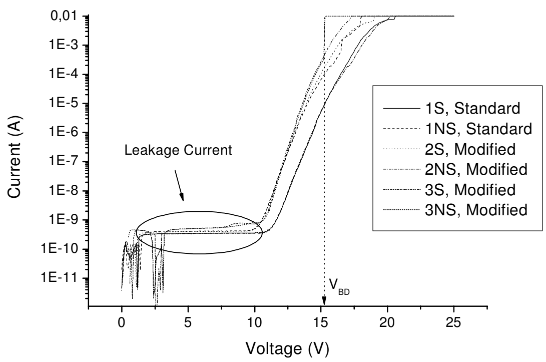

Figure 2: I-V curves from MOS capacitors for all analyzed samples.

The electric breakdown fields ($E_{BD}=V_{BD}/t_{ox}$) were determined and the average values of the V_{BD} and E_{BD} are shown in Table 2. The average breakdown field values are between 11~15 MV/cm.

The leakage current of the devices was obtained in I-V curves, before the breakdown. Values around 400 pA were determined.

From these results, in terms of structure, we have good silicon oxide films.

Table 2: Average extracted parameters from I-V curves

Sample	Cleaning	V_{BD} (V)	E_{BD} (MV/cm)
1S	Standard	19.9	11.8
1NS	Standard	20.3	14.4
2S	Modified	17.4	11.2
2NS	Modified	20.7	15.0
3S	Modified	13.9	13.6
3NS	Modified	14.5	14.7

As shown in Table 2, the breakdown fields of sintered samples are lower for all three types of samples.

Figure 3 shows the percentage distribution of E_{BD} in the measured samples.

It is observed that few capacitors have low breakdown field. Good results were observed either in sintered or in non sintered cases for sample 3, that have the thinnest oxide.

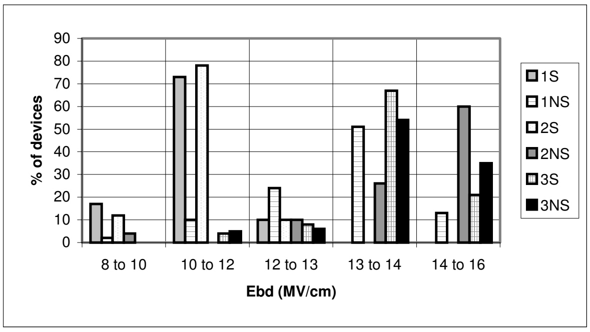

Figure 3: Percentage distribution of E_{BD} in the measured devices at all samples.

4. CONCLUSION

It was shown that the proposed alternative cleaning, that uses fewer chemicals, is as effective as the standard cleaning. However, Qss/q values of 10^{11} cm^{-2} were higher than the expected ones (~10^{10} cm^{-2}). More studies still need to be carried out in order to lower the Qss/q values for both cleanings.

REFERENCES

[1] - Sze S.M.; Physics of Semiconductor Devices; 2nd ed.; New York ; Wiley; 1981.

[2] - Singer, P.H. Trends in wafer cleaning. Semiconductor International, v. 15, n. 13, p. 36-39, 1992.

[3] - Ohmi, T; Miyashita, M.; Itano, M.; Imaoka, T.; Kawanabe,I. Dependence of thin-oxide films quality on surface microroughness. IEEE Trans. on Electron Devices, v. 39, n. 3, p. 537-45, 1992.

[4] – Martino, J. A., Pavanello, M.A., Verdonck, P.B., Caracterização Elétrica de Tecnologia e Dispositivos MOS, 2003.

ACKNOWLEDGMENT

FAPESP for financial support.

Dr. Leandro Zeidan Toquetti from LSI-USP for support in the fabrication processes.