TEST STRUCTURES TO EVALUATE A CELL LIBRARY

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ABSTRACT

This paper presents some kinds of test structures for propagation delay and power characterization in cell libraries. Due to the limitations of the instruments for electrical measurements directly done on the silicon, the measurement process needs a particular test structures set and a correct methodology of time analysis. The proposed structures, as well as the measurement methodology, are described in this work.

1. INTRODUCTION

The validation process of a library cell in silicon is one of the most important steps in projects of integrated circuits [1]. This step evaluate if the physical cell behavior is approximately the same previously characterized in the simulation process. In this point are made logic verification of combinatorial cells, proving them to be fully functional, and delay and power characterization of cells

The focus of this work is purpose a strategy to validate and characterize logic cell libraries, through test structures and benchmark circuits, due to measurements problems that will be described in the Section 2.

2. MEASUREMENT PROBLEMS

The measurement problems are commonly generated by impedance probe equipments and, consequently, it will affect the gotten results from circuit [2]. For these reasons, the methodology of measurement of the time delay used in the structures of this paper is indirect the time delay (Td) characterization is obtained from frequency measures.

3. PROPOSED TEST STRUCTURES

The presented test structures discussed in this paper using are:

3.1. Ring Oscillators Circuit

The Ring Oscillator (Fig. 1.) is an efficient way for measuring the average cell delay, (tdhl+tdlh)/2, avoiding the influence of external circuits and test environment parasitic factors [3]. This structure allows power measurement, if individual VDD pads are adopted and evaluation of delay variation for different power supply levels. In the Ring Oscillator the number of stages determines the signal frequency to be measured.

The increase of the number of stages reduces the influence of the inaccuracy factors. They may be caused by use of different oscillation enable cell (Nand or Nor), different load in the output node connected to an output buffer or irregular inter-cell routing.

Intrinsic capacitance of ring internal nodes can be modified using pass-transistors, in order to connect them to additional capacitances. The increase of intrinsic capacitance of ring internal nodes is used to reduce the frequency of ring oscillator.

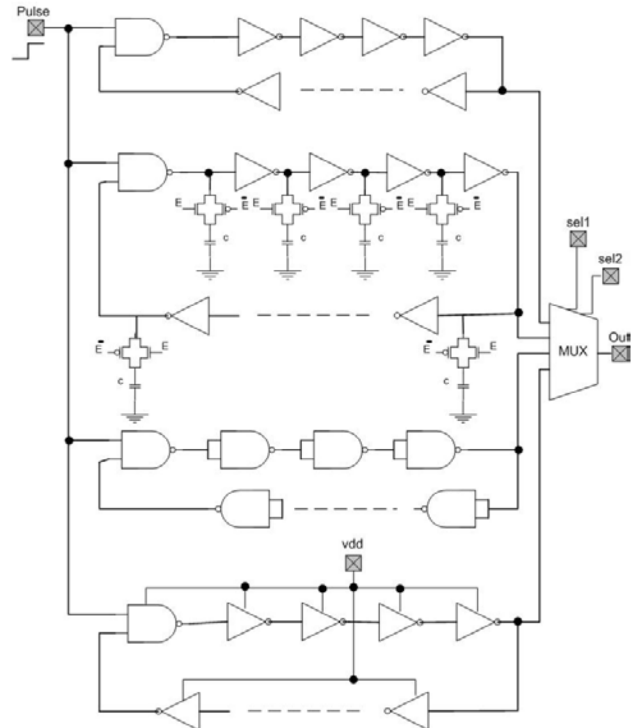

Fig.1. Schematic of ring oscilator structures.

3.2. Mixed-Cell Chains Circuit

This structure (Fig. 2) is a single-state FSM configuration, composed by independent logic paths (with different delays). It is used mainly to characterize 'long' logic paths and compare them to simulation timing analysis estimation [3].

The logic paths are switched through output multiplexer. States '0' and '1' are switched without influence of external input. The maximum frequency operation corresponds to single flip-flop timing (setup + delay) + logic path delay + multiplexer delay. No-

external input in the combinatorial path is required to set the initial state. It is determined by flip-flop set/reset inputs.

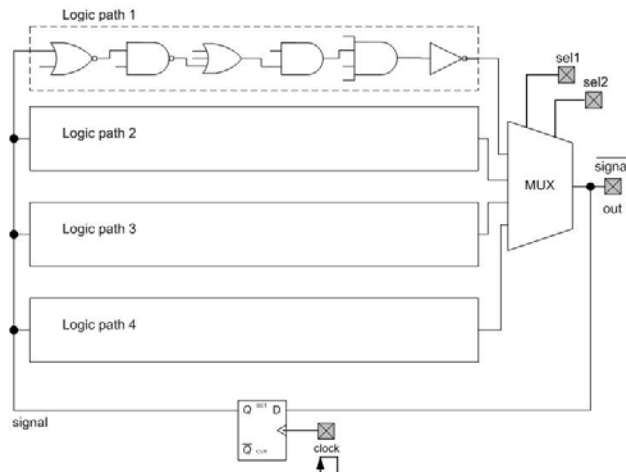

Fig. 2. Mixed-cell chains for timing evaluation (worst-case paths).

Other modifications can be added in the structure. External access to certain cell inputs should be interesting to verify different race conditions, dedicated power supply can be predicted for delay dependency to VDD and internal node capacitance can be selected through pass-transistor switch.

3.3. Sequential Cells Circuits

The Sequential Cells structures are used to verify the functionality of latches and flip-flops [3].

Latches and flip-flops have particular timing characteristics. In the latches are necessary the minimum enable signal width characterization and output-input and the output-enable delays analysis. In the flip-flops are necessary the maximum operation frequency, output-clock delay and setup and hold times characterizations.

These circuits allow verify power consumption and verify susceptibility to power supply variation too.

The configurations commonly used of this cells are frequency divider (asynchronous or ripple counter) (Fig. 3.), Latch Timing (Fig. 4.) in ring configuration (for delay measurement and minimum enable width analysis) and a specific Structure for Setup/Hold Characterization (Fig. 5.).

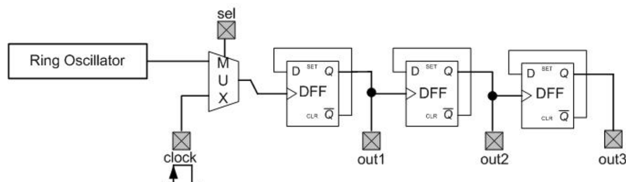

Fig 3. Frequency Divider for flip-flop timing and power analysis.

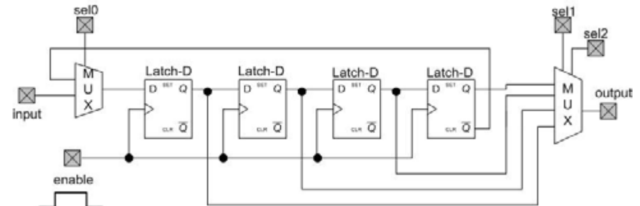

Fig. 4. Latch Timing for delay measurement and minimum enable width analysis.

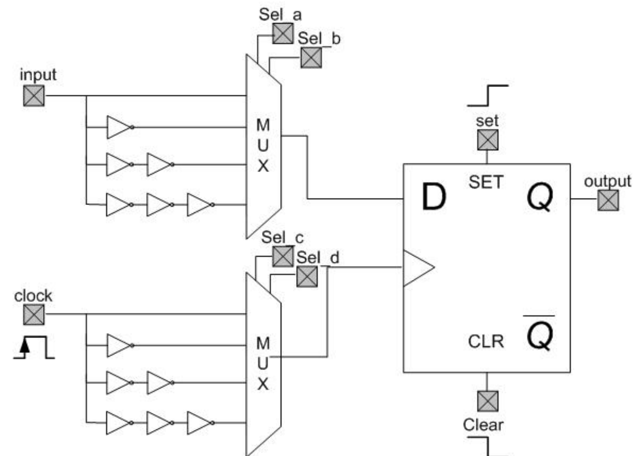

Fig. 5. Setup/Hold schematic for setup and hold timing delay analysis.

4. CONCLUSION

This paper presents some test structures and as they are used. We can observe that for each type of cell a characteristic type of circuit exists. Normally Ring Oscillators and Mixed-Cell Chains are used to characterize time delay, functionality and power consumption of combinatorial cells. Sequential Cells Structures are indicated to characterize power consumption and time delay in cells used in sequential circuits as latches and flip-flops. In addition, we can observe that indirect measurements demonstrate to be more trustworthy for the cell characterization of what direct measurements.

5. REFERENCES

[1] Mass, B.J. – "Algumas considerações para o projeto de osciladores em anel monolíticos.", Anais do II Simpósio Brasileiro de Microeletrônica, LME/UPUSP, pp 687 – 704, jul 1982.

[2] Long, Stephen I.- "Test Structures for Propagation Delay Measurements on High-Spees Integrated Circuits", IEEE Transactions on Electron Devices, vol. ED-31, NO. 8 august 1984.

[3] Ribas, R.P. – "Estruturas de teste para avaliação de uma boblioteca de células.", Anais do VII Simpósio Brasileiro de Concepção de Ciruitos Integrados, pp 270 – 281, 1992.