ENTROPY ENCODER ARCHITECTURES FOR H.264/AVC BASELINE PROFILE

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ABSTRACT

This paper presents the design of a hardware architecture for the Entropy Encoder of H.264/AVC video compression standard, considering the baseline profile. The entropy encoder is composed by two main blocks: Exp-Golomb encoder and CAVLC encoder. This paper presents the architectural design of these two blocks. The synthesis results targeting Xilinx FPGAs showed that the Exp-Golomb and CAVLC encoders reached a throughput of 10.2 million of samples per second for the Exp-Golomb encoder and of 117.62 million of samples per second for CAVLC encoder. The H.264/AVC baseline entropy encoder is being designed through the integration of these two encoders and preliminary results indicate that this solution will be able to process HDTV frames in real time.

1. INTRODUCTION

H.264/AVC is the latest video compression standard [1]. This work presents the architectural design of an Entropy Encoder block for this standard.

The H.264/AVC standard is divided in different profiles. The entropy encoder in the baseline profile uses two main tools to allow a high data compression: the Exp-Golomb encoding and Context Adaptive Variable Length Encoding (CAVLC) [2], as presented in Figure 1. The syntactic elements of each macroblock are entropy encoded using context adaptive variable length encoding (CAVLC) for residual information and Exp-Golomb codes for other coding units.

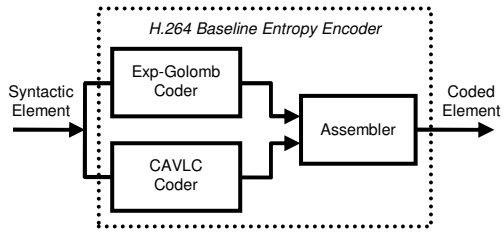

Figure 1. Baseline profile entropy encoder

2. EXP-GOLOMB ENCODER ARCHITECTURE

Exp-Golomb encoder architecture was designed through the implementation of a finite state machine connected with two ROM memories, as is presented in Figure 2.

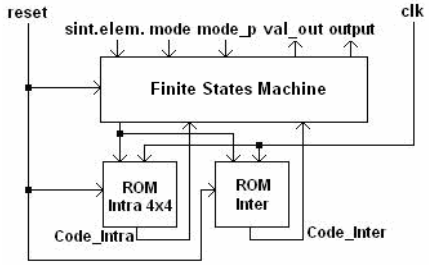

Figure 2. Exp-Golomb encoder block diagram

The input this architecture has 10 bits and the output has 1 bit. The output is delivered in an asynchronous way and the signal *val_out* indicates when an output is valid. The minimum latency this architecture is of two clock cycles.

3. CAVLC ENCODER ARCHITECTURE

The architecture designed for CAVLC encoder was designed through seven main blocks and five ROM memories. The main blocks are: *NC*, *Calc_Info*, *Control*, *PreMont_TCoeff_T1s*, *Levels*, *TotalZeros*, *RunBefore_ZeroLeft* and *Assembler*, like is shown in Figure 3. This architecture was designed in a pipeline with three stages to increase its performance. The input samples of the encoder use 9 bits and the output coefficients use 32 bits. The output is delivered in an asynchronous way and the signal *ok_Mont* indicates when an output is valid and its minimum latency is of 44 clock cycles.

4. SYNTHESES RESULTS

The syntheses of the Exp-Golomb encoder and the CAVLC encoder architectures were targeted to the Xilinx Virtex-II 2V8000 FPGA.

Table 1. Syntheses Results

Architecture	LUTs	Frequency (MHz)	Throughput (Msamples/s)
Exp-Golomb Encoder	341	122.76	10.2
CAVLC Encoder	3,137	117.62	117.62
Entropy Encoder *	3,500	100	100

* Estimated values — Device 2V8000

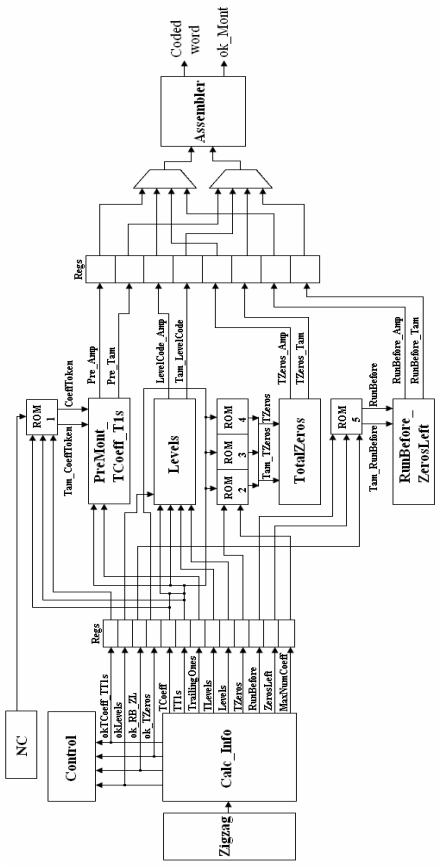

Figure 3. CAVLC encoder block diagram

The synthesis tool used was the Xilinx ISE. These results are presented in Table 1.

The integration of the Exp-Golomb encoder and CAVLC encoder architectures is being designed. Preliminaries results indicated that the complete baseline entropy encoder will reach a throughput near to 100 million of samples per second, allowing the coding of HDTV videos (1920x1080 pixels) in real time.

5. COMPARISONS WITH RELATED WORKS

There are a few papers published about the baseline entropy encoder of H.264 video compression standard. One paper related to the Exp-Golomb encoder [3] was found, but it was not possible to realize a complete analysis of this work once the number of inputs processed per clock cycle was not informed.

Three papers related to CAVLC encoder [4] [5] [6] were found. The architecture designed in this paper has a throughput up to 4.3 times lesser than the architecture presented in [4], but the architecture presented in [4] consumes 27 times more hardware resources considering the same target device. The architecture proposed in this paper presented a throughput 17.4 times higher than that presented in [5] and used approximately twice less hardware resources. The comparison with [6] shows that the architecture designed in this paper reached a throughput approximately 2 times higher than that presented in [6]. A comparison with paper [6] in terms of hardware consumption was not viable, once the target technologies are different (FPGA versus standard-cells). In function of these comparisons, it is possible to conclude that the CAVLC encoder architecture designed in this paper has interesting profits in relation to other published works.

6. CONCLUSIONS AND FUTURE WORKS

This work presented the design of architectures for the entropy encoder of the H.264 video compression standard, considering the baseline profile.

From the comparison of these results with related works, it is possible to conclude that the Exp-Golomb encoder and CAVLC encoder reached interesting results.

The integration of Exp-Golomb and CAVLC encoders architectures was not finished yet, but some estimates were generate considering the preliminary results. These estimates indicate that the complete baseline entropy encoder will use near to 3,500 LUTs, reaching a throughput near to 100 million of samples per second. This throughput is enough to process HDTV videos (1920x1080) in real time.

The conclusion of the Exp-Golomb and CAVLC encoders integration is planned as future work. With the integration finished, a complete entropy encoder for the baseline profile of the H.264 standard will be available.

7. REFERENCES

[1] INT. TELECOMMUNICATION UNION. ITU-T Recommendation H.264 (03/05): Advanced Video Coding for Generic Audiovisual Services, 2005.

[2] I. Richardson, *H.264 and MPEG-4 Video Compression*, Chichester: John Wiley and Sons, 2003.

[3] W. Di, G. Wen, H. Mingzeng and J. Zhenzhou, “An Exp-Golomb Coder and Decoder Architecture for JVT/AVS”, IEEE Trans. on Circuits and Systems for Video Technology, v. 2, n. 21-24, p. 910-913, 2003.

[4] I.Amer, W. Badawy and G. Jullien, “Towards MPEG-4 Part 10 System on Chip: a VLSI Prototype for Context Based Adaptive Variable Length Coding (CAVLC)”, In: IEEE Workshop on Signal Processing Systems, p. 275-279, 2004

[5] E. Sahin and I. Hamzaoglu, “A High Performance and Low Power Hardware Architecture for H.264 CAVLC Algorithm”, In: 13th European Signal Processing Conference, 2005.

[6] C. Chien, K. Lu, Y. Shih and J. Guo, “A High Performance CAVLC Encoder Design for MPEG-4 AVC/H.264 Video Coding Applications”, In: Int. Symp. on Circuits and Systems, p. 3838-3841, 2006.