CHARGE DISTRIBUTION IN TRIPLE-GATE DEVICES AT THRESHOLD VOLTAGE

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ABSTRACT

This paper describes the results of some three-dimensional simulations of triple-gate devices. The electron concentration along different cut lines is analyzed for some channel doping levels and some different channel widths at threshold voltage.

1. INTRODUCTION

As the industry get closer to scale limits of classical planar structures, new alternatives are being developed. One possible approach is the creation of multiple gate transistor designs. This kind of structure improves the solution of short-channel effects and increment current drive [1]. An identified effect in multiple-gate devices is the volume inversion [2], where carriers are distributed in the center of the film and not only near the Si/SiO_2 gate interface. This effect results in superior transconductance [1]. These new concepts brought new challenges and new fields to research. One of them is the corner effect [3]. In simulated devices it is possible to verify this effect and analyze it for different levels of doping concentrations and different device dimensions. Some research has been made on how to control this effect by controlling the corner curvature radii or reducing the doping concentration at the channel [4].

2. SIMULATED DEVICE

Figure 1.a shows the triple-gate simulated device. This transistor presents gate oxide thickness (t_{OX}) of 3 nm for the three gates, buried oxide thickness (t_{BOX}) of 200 nm and interface charge density of $3.0x10^{10}$ cm^{-2}. Tungsten, a near midgap material was adopted for the gate material. The channel was designed as a symmetrical square (H=W). The channel length (L) of 200nm was adopted for all simulations.

Na (cm^{-3})	H=W (nm)		
	30	50	70
10^{16}	0.3316 V	0.3214 V	0.3147 V
10^{17}	0.3602 V	0.3641 V	0.3697 V
10^{18}	0.4962 V	0.5414 V	0.5624 V
10^{19}	0.9721 V	1.0490 V	1.0838 V

Table 1 – Table of threshold voltage for simulated devices.

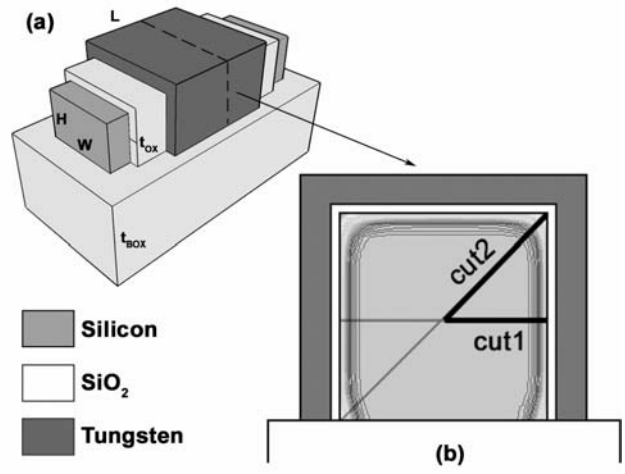

Figure 1: (a) Triple-gate simulated device, t_{OX} - gate oxide thickness, t_{BOX} – buried oxide thickness, W – channel width, H – channel height and L – channel length. (b) Transversal cut at the middle of channel and two cut lines – cut1 and cut2

The work was developed with 12 different transistors in Atlas simulator version 5.10.0.R. Four different silicon doping concentrations (N_a) were used: $10^{16}cm^{-3}$, $10^{17}cm^{-3}$, $10^{18}cm^{-3}$ and $10^{19}cm^{-3}$. Three symmetrical channel sizes (H=W) were adopted: 30nm, 50nm and 70 nm. The threshold voltage (V_{TH}) was obtained from the drain current (I_d) versus gate voltage (V_G) curve extrapolation for V_d=10mV. See results in Table 1. The "extrapolated" V_{TH} was calculated by the interception of tangent and horizontal axis [5]. Impact ionization models were considered even for low drain voltages. Quantum effects were not considered.

3. CHARGE DISTRIBUTION AT THRESHOLD VOLTAGE

Using the values of V_{TH} from Table 1, cross sections at the center of each transistor were obtained as showed in Figure 1.b and curves of electron concentration versus normalized distance from the center to the interface Si/SiO_2 were traced. Two different cut lines were adopted. One horizontal cut from the center of channel to the interface Si/SiO_2 (cut1) and a second, diagonal from center to the corner (cut2).

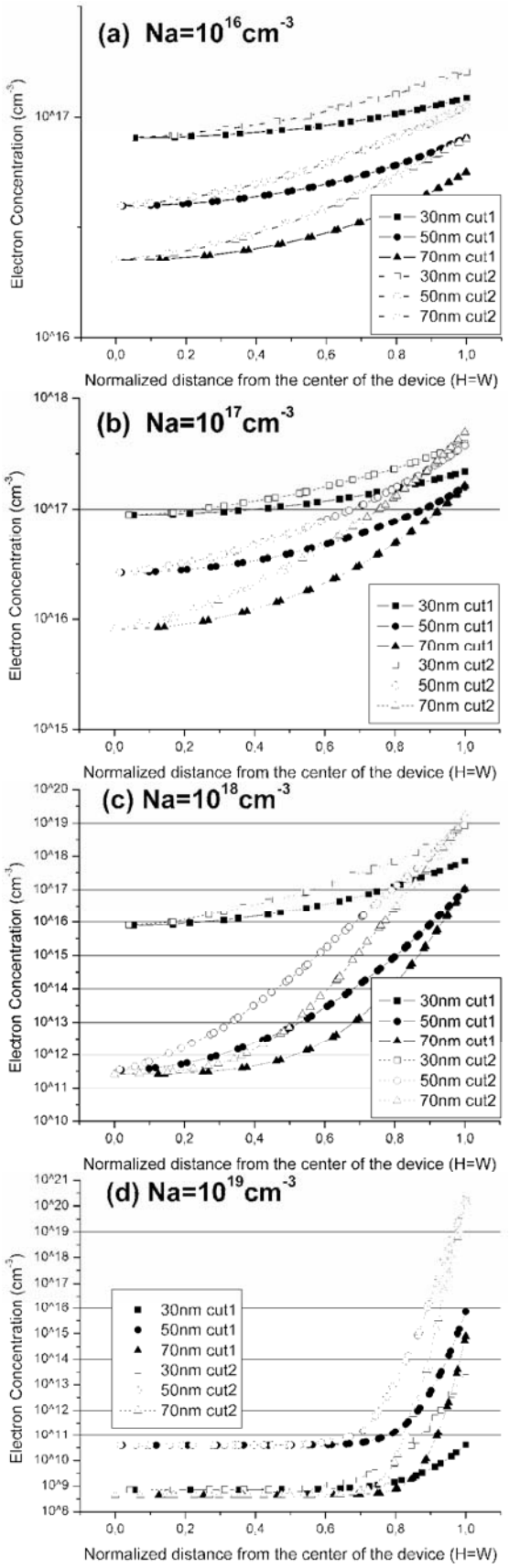

Figure 3 – Curves of electron distribution versus normalized distance for three symmetrical channel sizes (H=W) and two cut lines at threshold voltage, classified by doping levels. (Note: for better observation scales are different in "y" for each plot.)

Curves from Figure 3 were traced from the previously defined cut lines for all transistors and classified by doping concentrations. The distances from the center were normalized, so 0 (zero) represents the center of the device and 1 (one) is the gate Si/SiO_2 interface. The corner effect can be observed by comparing the filled-marker (cut 1) to the non filled-marker curves (cut 2). It can be seen that electron concentration is higher at the corners. The influence of the doping level can be analyzed by comparing Figures 3.a through 3.d. Figure 3.a presents extracted curves from devices with doping concentration of $10^{16}cm^{-3}$. It can be seen that electron concentration curves of cut 1 and cut 2 are quite near one from another for the three device widths. As the doping level increases (Figures 3.b, c and d) the distance between the concentration values of cut 1 and 2 also increases, what shows a strong dependence of corner effect on the doping level. Figure 3.d ($10^{19}cm^{-3}$) shows a difference of almost three decades in the electron concentration near the interface Si/SiO_2 for the cut lines cut1 and cut2. The channel height and width also influence the corner effect: for larger devices the corner effect is stronger. In Figure 3.d it was observed that there was small electron concentration near the center of the channel, due to higher doping. This means that the volume inversion mechanism is less meaningful in this case. Based on that, one could infer that the triple-gate device works in a similar way that would work three independent single-gate devices.

4. CONCLUSION

The three-dimensional simulation study of triple-gate devices showed that low doping concentrations and reduced channels sizes (H=W) reduce the strength of the corner effects. Also, the volume inversion effect can be clearly observed for lower doping levels and smaller devices. Further study is proposed using quantum effects and different channel sizes (L).

5. REFERENCES

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