STUDY OF HIGH TEMPERATURE INFLUENCE ON HIGH FREQUENCY C-V CHARACTERISTICS OF MOS CAPACITOR

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ABSTRACT

The study of MOS capacitor capacitance versus voltage (C-V) curves in AC high frequency analysis is performed for temperatures from room temperature up to 573K. Bi-dimensional simulations were performed to evaluate the analysis of MOS capacitor structures with different substrate doping concentration values and different insulator layer thicknesses.

1. INTRODUCTION

The increasing utilization of MOS devices in applications involving high temperature environments has demanded for further knowledge on components behavior up to 573K.

The study of C-V curves behavior in harsh environmental conditions is subject of great interest for electronic controls employed on avionics, internal combustion engines and geothermal oil wells applications, which are currently the most demanding markets for reliable high temperature silicon based devices [1, 2, 3, 4].

It is a fact that the overall cost of electronic devices applied to automobiles and airplanes can be expressively reduced if they can operate directly in hot areas [1, 2, 3, 4]. This would also eliminate the necessity of insulation and cooling mechanisms or devices to maintain the temperature within the limits tolerated by silicon, currently around 398K [1].

The MOS capacitor was selected to be studied in this context, especially due to its simple structure and presence in almost every MOS device, being the elementary MOS transistor structure.

The MOS capacitor structure is shown in figure 1, which one is composed by a metal gate, an insulator layer and a semiconductor substrate which enables, through the simulated capacitance versus gate voltage curves, the study of parasitic effects caused by the temperature increases.

In this paper, the results presented were obtained through the bi-dimensional simulator ATLAS [5]. The high frequency C-V curves were analyzed for a temperature range starting at room temperature (300K) and raised up to 573K.

For each group of curves, two parameters were analyzed in order to demonstrate the temperature influences on C-V characteristics: the silicon substrate doping concentration and the oxide layer thickness.

2. DEVICE CHARACTERISTICS

The MOS capacitor used in this work is composed by a poly-silicon N+ gate, an SiO_2 insulator layer t_{ox}= 2.5 nm, a P silicon substrate layer t_{Si}= 150 nm and the substrate doping concentration being N_A= 5x10^{17} cm^{-3}, as presented in figure 1.

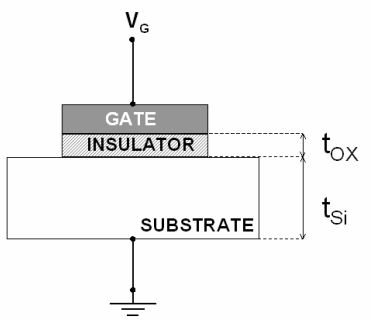

Figure 1 – MOS Capacitor structure.

A DC voltage varying from -3V to 3V was applied to the gate (V_G) and the AC analysis was performed using a 1 MHz frequency.

Simulations were performed for different temperatures with an interval of 50K between each simulation and the C-V curves obtained for room temperature was used as the mainstream for all the comparative analysis.

3. SIMULATION RESULTS

The first C-V curve obtained is shown in figure 2 where it can be observed that, for positive voltages applied in the capacitor gate (V_G > 0V), the curve presents a deviation from typical high frequency C-V curve when it is operating up to 473K. This behavior tends to approach to the typical low frequency C-V curves, although the frequency was maintained constant at 1 MHz during all simulations. Another point to be further investigated is the second peak observed in the C-V curves when V_G is larger than 0V and for the temperature being 573K.

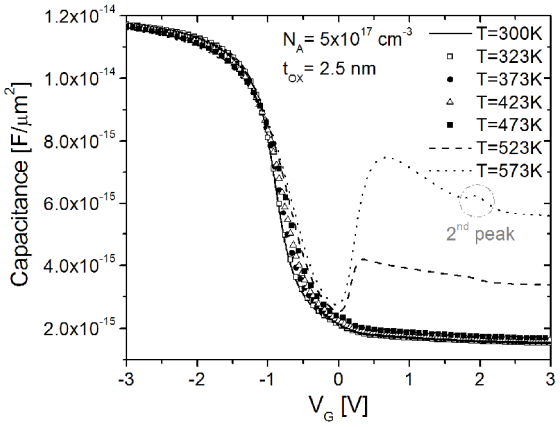

Figure 2 – C-V curves for N_A= 5x10^{17} cm^{-3} and t_{OX}= 2.5 nm operating at high temperatures.

In order to investigate the deviation observed in the MOS C-V curves at high temperatures, the substrate doping concentration N_A influence was analyzed for the same structure operating at same conditions. Some results are shown in figures 3 and 4, for N_A being $5x10^{15}$ cm^{-3} and $5x10^{19}$ cm^{-3}, respectively.

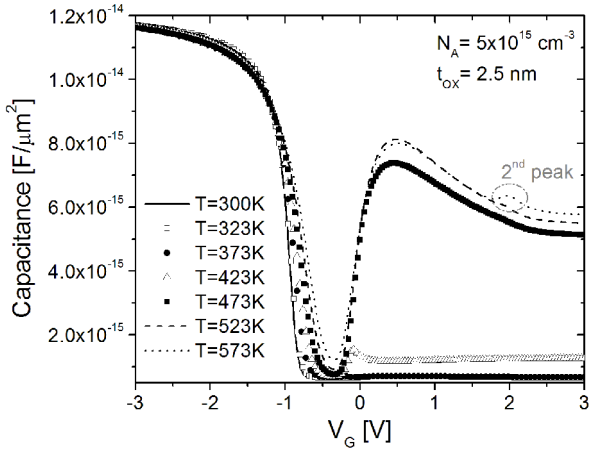

Figure 3 – C-V characteristic curves for N_A= $5x10^{15}$ cm^{-3} and t_{OX}= 2.5 nm.

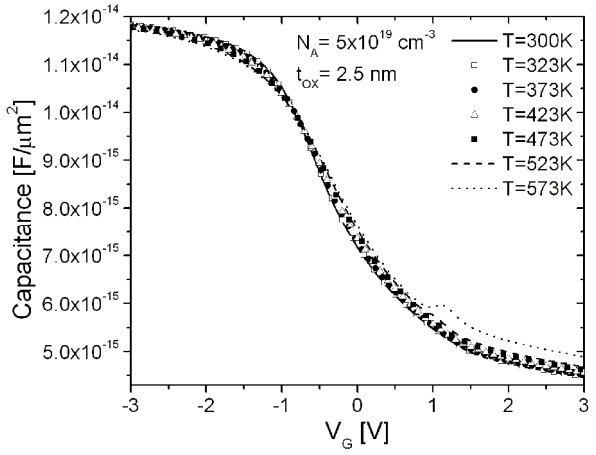

Figure 4 – C-V characteristic curves for N_A= $5x10^{19}$ cm^{-3} and t_{OX}= 2.5 nm.

From the results, it is possible to observe that the doping concentration variation influences directly in the C-V curves behavior as the temperature increases. It can be seen that as N_A increases, the deviation point appears at higher temperatures, as following. For example, figure 4 shows that for N_A= $5x10^{19}$ cm^3, only at 573K the capacitance increase effect is present for V_G > 0V. Similar behavior is also observed for the curves shown in figure 3, where N_A= $5x10^{15}$ cm^{-3}. In this case, the deviation effect appears earlier (at 423K) when compared to the results presented in figure 2.

Besides that, from the results showed in figures 2 to 4, it can be seen that the second peak observed in the C-V curves for V_G >> 0V also depends on substrate concentration and temperature, meaning that for higher doping concentrations, the necessary temperature for the MOS capacitor to presents this effect would be higher than the upper temperature limit range analyzed in this paper.

Further investigation was then performed for different oxide layer thicknesses in order to understand the high frequency capacitance behavior at high temperatures.

Figures 5 to 7 show the results concerned to the MOS capacitor with t_{ox}= 4 nm. The overall C-V curve tendency is similar to the one observed for t_{ox}= 2.5 nm, which demonstrates that the oxide film thickness is not a parameter that can neither degenerate nor improve the C-V characteristic behavior at high temperatures operation.

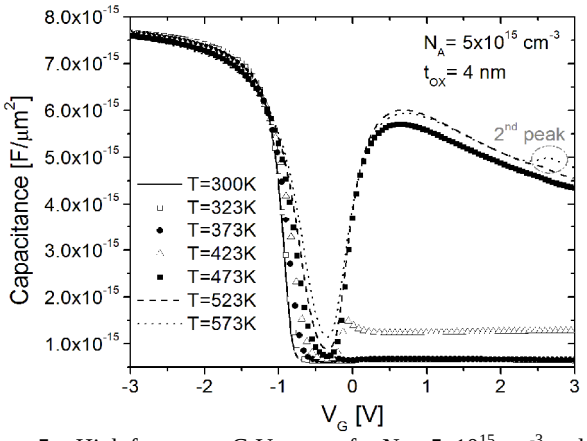

Figure 5 – High frequency C-V curves for N_A= $5x10^{15}$ cm^{-3} and t_{OX}= 4 nm.

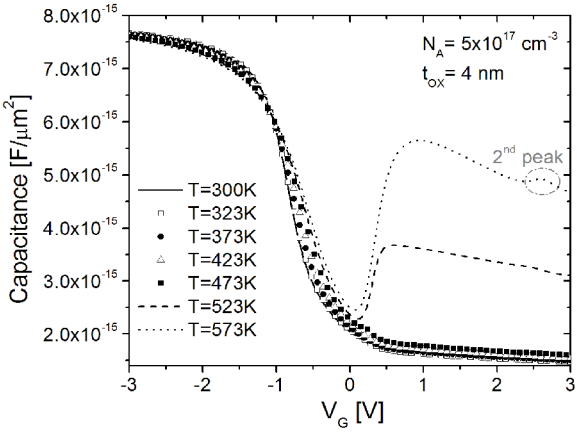

Figure 6 – High frequency C-V curves for N_A= $5x10^{17}$ cm^{-3} and t_{OX}= 4 nm.

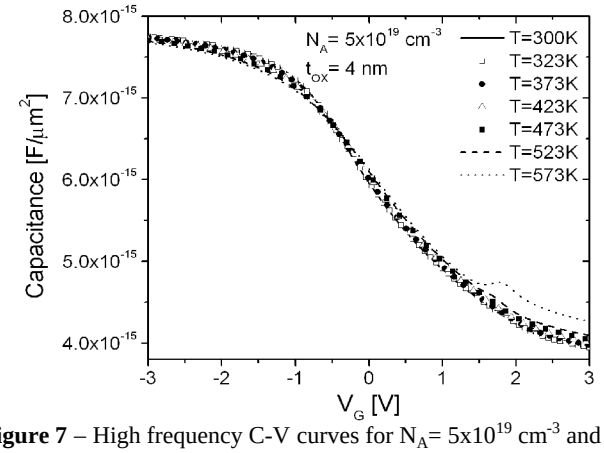

Figure 7 – High frequency C-V curves for N_A= $5x10^{19}$ cm^{-3} and t_{OX}= 4 nm.

Similar results were observed for the MOS capacitors with t_{ox}= 2 nm, as it can be seen in figures 8 to 10.

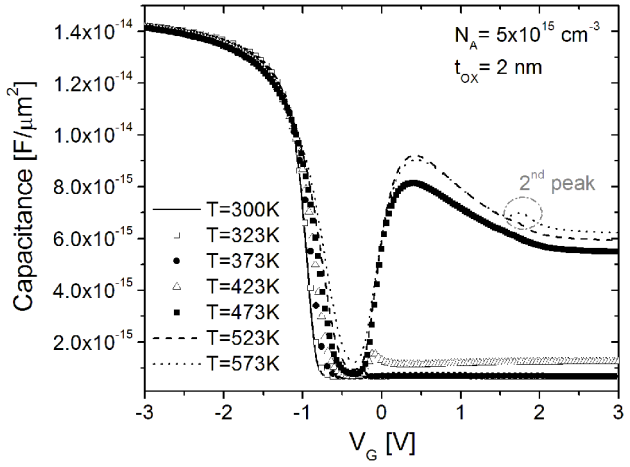

Figure 8 – C-V curve for N_A= 5x10^{15} cm^{-3} and t_{OX}= 2 nm operating at high frequency.

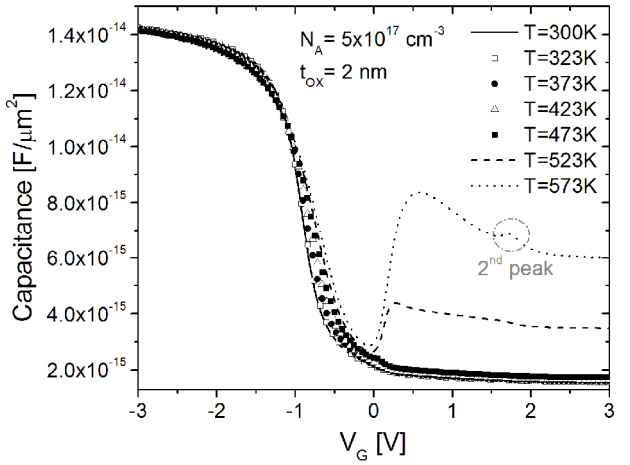

Figure 9 – C-V curve for N_A= 5x10^{17} cm^{-3} and t_{OX}= 2 nm operating at high frequency.

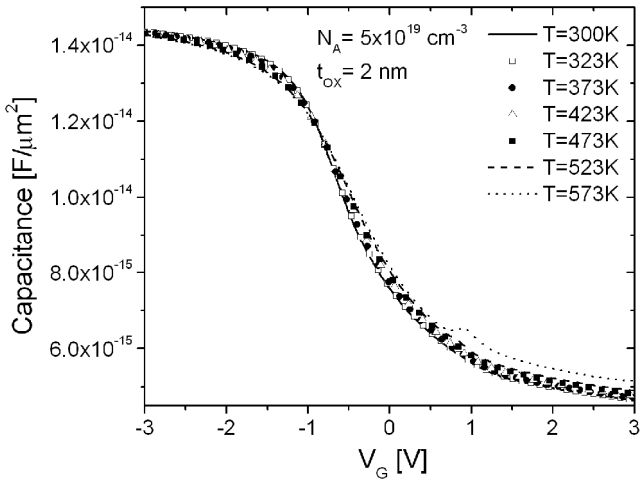

Figure 10 – C-V curve for N_A= 5x10^{19} cm^{-3} and t_{OX}= 2 nm operating at high frequency.

4. RESULTS AND DISCUSSIONS

The C-V curves deviation observed in this work, when compared to the expected behavior when V_G > 0V and for temperatures higher than 423K, is due to some silicon physical limits.

One of the reasons for these electrical characteristics which changes with the temperature increases, is the silicon bandgap reduction. This effect originates an electrical conductivity degradation in the device operation as the temperature increases [6, 7, 8].

The electrical conductivity degradation is mainly due to the substrate intrinsic carriers concentration that at high temperatures, rises significantly enough to overcome any other carrier concentration on silicon substrate, as expected by equation (4.1). Although the doping concentration, that was originally implanted on the substrate during the device fabrication, is higher than the intrinsic silicon concentration at room temperature, when an elevated temperature is applied on the device, the influence of silicon intrinsic carriers on conductivity is significantly high to degenerate the device's electrical operation behavior [7, 8].

$$n_i = \sqrt{N_c . N_v . e^{-Eg/2kT}} \qquad (4.1)$$

where:

n_i – intrinsic carrier concentration
N_C – effective density of states in the conduction band
N_V – effective density of states in the valence band
Eg – energy bandgap of semiconductor
k – Boltzmann's constant
T – absolute temperature

The electrical conductivity difficulty is clearly observed in the simulated curves as shown in figures 3, 5 and 8 for N_A= 5x10^{15} cm^{-3}. The C-V curves present strong deviation from the typical high frequency C-V behavior and quite high capacitance values for V_G > 0 V. In addition, for N_A= 5x10^{19} cm^{-3}, the conductivity difficulty in the substrate is almost inexistent as shown in figures 4, 7 and 10.

Due to this physical limitation, many researchers are studying other possible semiconductor materials like SiC (silicon carbide) that presents wider bandgap and, consequently a lower intrinsic carrier concentration when exposed to 573 K, becoming more reliable and suitable for high temperature operation applications [7, 8, 9, 10].

Regarding the oxide layer thickness, the simulation results show that this parameter has no significant influence on MOS capacitor high frequency C-V curves at high temperatures. The analysis of the energy band diagram, that represents the simulated MOS capacitor presented in figure 11, demonstrates that both the Fermi potential at the semiconductor (ϕ_F) and the depletion region maximum value (d_{max}) do not depend on the oxide layer thickness, which is confirmed by equations (4.2) and (4.3) where the parameter t_{OX} has no influences [11, 12, 13].

$$d_{max} = \sqrt{\frac{2.\varepsilon_{Si}.2\Phi F}{q.N_A}} \qquad (4.2)$$

$$\Phi F = \frac{k.T}{q} \ln \frac{NA}{ni} \qquad (4.3)$$

where:

d_{max} – depletion layer maximum width
ε_{Si} – permittivity of silicon
ϕ_F – Fermi potential of semiconductor
q – electron charge magnitude
k – Boltzmann's constant
T – absolute temperature

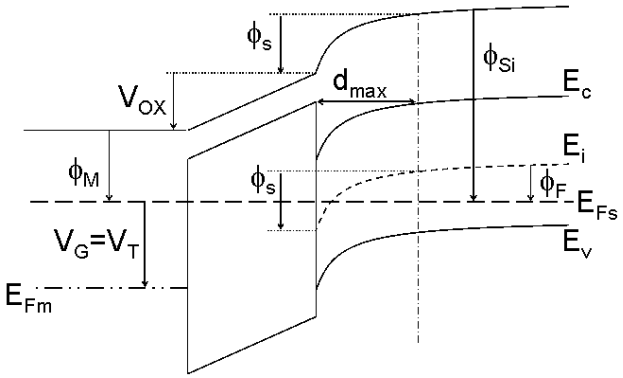

Figure 11 – The MOS capacitor with P substrate energy band diagram.

Therefore, this confirms that C-V curves behavior observed for high temperature application does not depend on t_{ox} thickness. However, accurate investigations will be done in order to understand the mechanisms that appear in MOS structure operating in such conditions.

5. CONCLUSIONS

These initial studies of the MOS capacitor operating at high temperatures indicate that the doping substrate concentration influences on high frequency C-V curves behavior.

It was observed that for the gate voltage higher than 0V, the capacitance values change as the temperature increases. Besides that, it was also noticed that for lower doping substrate concentration the high frequency C-V curves behavior changes, indicating that the capacitance due to the substrate significantly influence in these conditions (bias and temperature).

The second peak that was observed in the high frequency C-V curves operating at high temperatures needs an accurate studies in order to elucidate the physical effects that create this deviation observed in MOS capacitor operating at such conditions.

6. REFERENCES

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