THE HALO INFLUENCE ON PD SOI N-MOSFETS AT LOW TEMPERATURE OPERATION

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ABSTRACT

This work analyzes the partially depleted (PD) Silicon-On-Insulator (SOI) nMOSFET's devices behavior with and without HALO implantation, varying the operating temperature from 300K down to 100K, for devices with channel length from 10µm to 0.13µm. It is also verified, the HALO implantation doping concentration variation, from $8.0x10^{17}cm^{-3}$ to $4.0x10^{18}cm^{-3}$. The study was based on results of two-dimensional numerical simulations and is supported by experimental results. The studied parameters were threshold voltage and subthreshold slope. The HALO implantation increases the threshold voltage in devices and when the devices are operating in low temperature the threshold voltage is higher. The subthreshold slope decreases because this parameter suffers the direct influence of the temperature.

1. INTRODUCTION

Nowadays, the SOI MOSFET's devices are being used in digital circuit's application. The digital circuits are indeed attractive because of their enhanced performance (higher speed, low power and low voltage) and scalability. The SOI devices are most attractive in the highly competitive domain of low power/voltage circuits [1].

The SOI device offers the possibility to achieve a quasi-ideal subthreshold slope (60 mV/decade at room temperature), hence a threshold voltage below 0.3 V. Low leakage currents limit the static power dissipation, as compared to bulk Si, whereas the dynamic power dissipation is minimized by the combined effects of low parasitic capacitances and reduced voltage supply. It is possible to combining the digital and analogical circuits in the same technology [1].

When these devices operate at low temperature, there are an improvement of the electrical characteristics like the increase of the mobility of carriers, increase of the saturation velocity, the reduction of the subthereshold slope and the reduction of junction capacitance, beyond allowing higher drain current without the necessity to reduce the dimensions; however impact ionization became more critical [2].

In devices with short dimensions the output characteristics can be degraded due to the increase of the leakage current and the short channel effect, then, with the purpose to reduce these effects a HALO concentration was implanted in the devices.

In SOI MOSFET devices with floating body, the body potential is higher and therefore cause some problems like the degradation of the saturation output conductance, due to the kink effect and the reduce of the breakdown voltage [3], but when there is a HALO implantation in these devices, it is possible to see an increase in the threshold voltage with the short channel effects.

The HALO implantation is give through an implantation of one high doping of boron [4], with the purpose to control the short channel effect on the submicrometer devices.

Figure 1 shows the structure with the implantation of the HALO in a SOI device.

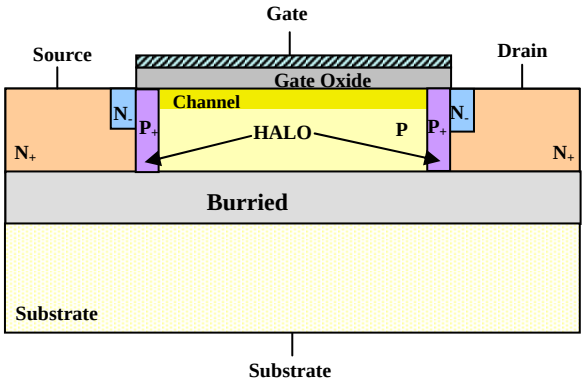


Figure 1: Structure of SOI nMOSFET with HALO.

The aim of this work is to analyze the impact of the HALO implantation in PD SOI MOSFET's, operating from room to low temperatures for a channel length varying from 10µm to 0.13µm.

2. DEVICES CHARACTERISTICS

The studied devices characteristics are: gate oxide (t_{oxf}), silicon film (t_{Si}) and buried oxide thicknesses (t_{oxb}) of 2.5 nm, 100 nm and 390 nm, respectively, and a channel doping concentration of $5.5x10^{17}$ cm^{-3}. The channel width (W) is 10 μm for the measured devices, while for the performed simulations the curves were obtained per unit width, since the simulations are two-dimensional. The channel length (L) ranged from 10μm to 0.13μm the source and drain doping concentration is $1.0x10^{20}cm^{-3}$, the low doped drain concentration (L_{DD}) is $5.0x10^{19}cm^{-3}$ and the used concentrations of the HALO implantation are: $8x10^{17}cm^{-3}$, $1x10^{18}cm^{-3}$, $1.2x10^{18}cm^{-3}$, $1.4x10^{18}cm^{-3}$, $1.6x10^{18}cm^{-3}$, $2x10^{18}cm^{-3}$, $3x10^{18}cm^{-3}$ and $4x10^{18}cm^{-3}$.

The two-dimensional numerical simulations were performed using the ATLAS simulator program and the considered models were the amount of carriers ionized, carrier mobility, carrier intrinsic concentration, generation and recombination carriers lifetimes and the perpendicular electric field [6].

3. RESULTS AND ANALYSIS

Several simulations were performed with the characteristics previously mentioned. Through these simulations, it was obtained the drain current (I_{DS}) as a function of the gate voltage (V_{GF}) curves. From the simulated curves some electrical parameters were extracted like threshold voltage and subthreshold slope.

The drain current as a function of the gate voltage curves had been extracted with a drain voltage (V_{DS}) of 25mV, with a variation gate voltage (V_{GF}) from -0.25 to 1.5V with steps of 10mV. The threshold voltage had been extracted from the second derivative method from these curves.

The threshold voltage for the devices PD SOI MOSFETs with HALO is given by [5], as it shows equation 1.

$$V_{th} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}} + 2.\Phi_F + \left(\frac{q.N_{aef}.x_{dmáx}}{C_{ox}} \right) \quad (1)$$

where: V_{th} is threshold voltage, Φ_{MS} is the work function, Q_{ox} is the gate oxide charge density, C_{ox} is the oxide capacitance, ϕ_F is the Fermi potential, N_{aef} is the effective doping concentration and x_{dmax} is the maximum depletion depth.

The semiconductor effective doping concentration is given by equation 2 [7].

$$N_{aef} = \frac{N_a(L - 2.L_{halo})}{L} + \frac{2.N_{halo}(L_{halo})}{L} \quad (2)$$

where: N_a is the substrate doping concentration, N_{halo} is the HALO doping concentration, L_{halo} is the halo width and L is the effective channel length .

Equations 3, 4 and 5 are given by [6].

$$\Phi_F = \frac{k.T}{q}.\ln\left(\frac{N_a}{n_i}\right) \quad (3)$$

where: k is the Boltzmann constant, T is the temperature and n_i is the intrinsic carrier concentration.

$$n_i = 3{,}9x10^{16}.T^{\frac{3}{2}}.e^{-\left(\frac{E_g}{2.k.T}\right)} \quad (4)$$

$$x_{dmáx} = \sqrt{\frac{4.\varepsilon_{Si}.\Phi_F}{q.N_a}} \quad (5)$$

where: ε_{Si} is the silicon permittivity.

The figure 2 shows the threshold voltage (V_{th}) as a function of the channel length variation for devices with and without HALO implantation, for different HALO doping concentration at room temperature.

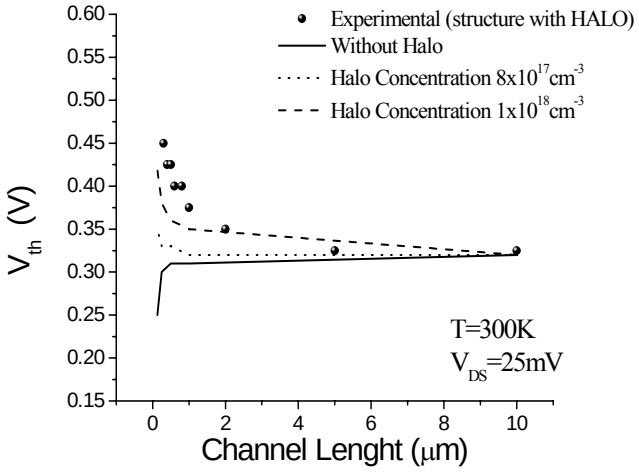


Figure 2: Threshold voltage versus channel length for devices with and without HALO, for different HALO doping concentration at room temperature.

The experimental results with HALO doping concentration of $1.0x10^{18}cm^{-3}$ is also showed in figure 2.

Comparing the experimental and simulated results, the same tendence is observed.

It is also possible to note that in PD SOI MOSFET device without HALO presents lower threshold voltage when the channel length of device is decreased. It is due to the small gate control of the total charges, i.e., increases the source and drain depletion region influence on the total charges control.

In devices with HALO, the threshold voltage increases with the reduction of the channel length owing

to the interaction between the source and drain charges which rise the effective channel doping.

In order to observe the behavior of threshold voltage with variation of HALO concentration, it was performed simulations with several values of doping concentration.

Figure 3 shows the threshold voltage (V_{th}) as a function of temperature for devices with and without HALO, with channel length of 0.13µm, varying the HALO doping concentrations.

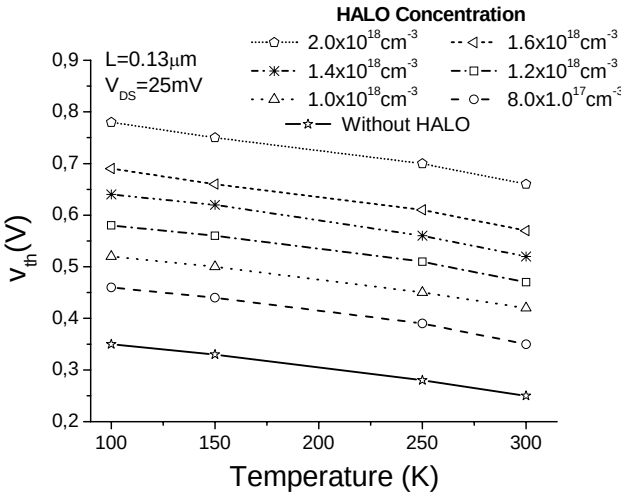


Figure 3: Threshold voltage versus temperature, for devices with channel length of 0.13 µm, with and without HALO, varying the HALO doping concentration.

Figure 3 shows that there is an increase of threshold voltage with the reduction of the temperature, because of the Fermi level potential increase.

On the other hand it can be also observed that the threshold voltage increase while the HALO doping concentration is raised, whereas the effective channel doping concentration besides rises.

Figure 4 was obtained with the decrement at the low temperature (LT) and the room temperature (RT), as shows the equation 6.

$$\Delta V_{th}=V_{th}(LT)-V_{th}(RT) \quad (6)$$

Figure 4 represents the variation of the threshold voltage (ΔV_{th}) in function of the temperature, for several HALO concentrations for a drain voltage (V_{DS}) of 25mV.

Although in the first analysis in the figure 3, its suggests that the increase of threshold voltage as a function of the temperature is practically parallel, but if we observe the threshold voltage for the same temperature, it can be noted that while HALO concentration increase, the threshold voltage also increase, due to Fermi level potential increase.

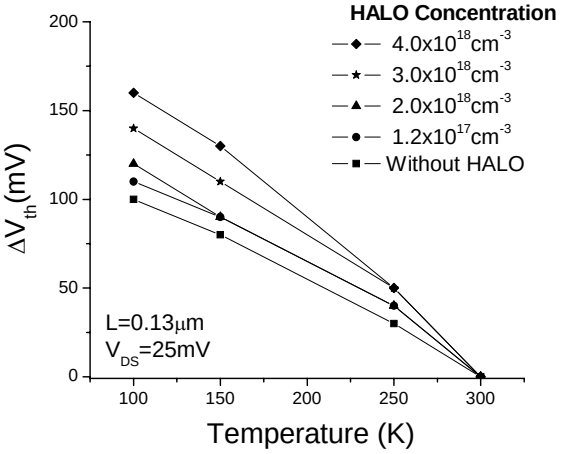
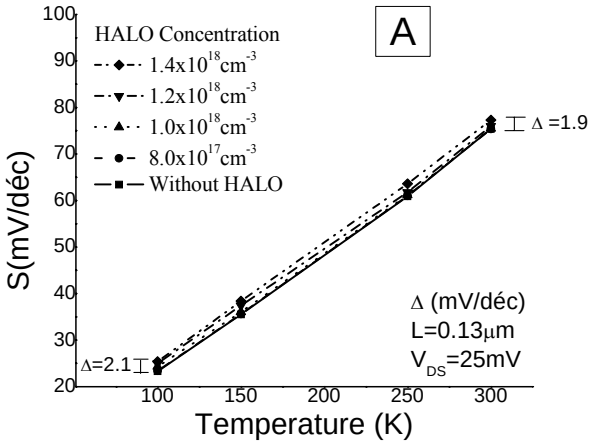


Figure 4: Variation of the threshold voltage versus temperature, for devices with and without HALO, varying HALO doping concentration.

However, in the figure 4 it is observed that the variation of the threshold voltage in devices PD SOI MOSFET without HALO is lower than in the devices with HALO at all temperatures (300K down to 100K) due to the effective carriers concentration of devices without HALO to be low, resulting in a lower influence in the Fermi potential.

The figure 5 shows the subthreshold slope (S) in function of temperature curve for several HALO doping concentrations for devices with channel length of 10µm (A) and 0.13µm (B).



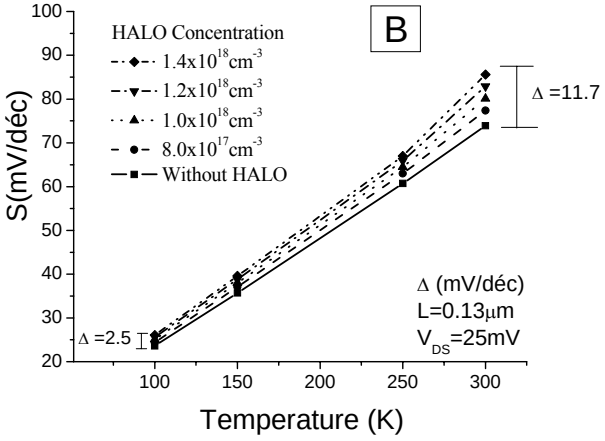


Figure 5: Subthreshold slope versus temperature, for devices with channel length of (A) 10μm and (B) 0.13μm.

Figure 5(A), shows the subthreshold slope as a function of temperature for a device with channel length of 10μm for several HALO doping concentration, where can be noted that those devices has a subthreshold slope practically constant, as much at room temperature as at low temperature, because the HALO does not have influence on devices with the long channel length as expected. This linear behavior of subthreshold slope with temperature is due to the interfaces trap density was neglected.

Figure 5(B), shows the subthreshold slope as a function of temperature for a device with channel length of 0.13μm for several HALO doping concentration, it is possible to note that in device at room temperature the variation of subthreshold slope is higher than in devices at low temperature, owing to the reduction of the maximum depletion depth and the rise of the depletion charges capacitance

Then can be concluded that PD SOI MOSFET devices with HALO present a higher subthreshold slope when operate at low temperature (100K), it occurs because of the increase of body effect and the short channel effect is minimized. This effect becomes higher when the HALO doping concentrations is increased.

4. CONCLUSION

With the HALO implantation in the devices, it was possible to note that the parameters studied in this work present a significant improvement in the devices, mainly in the device PD SOI nMOSFET with short channel.

The threshold voltage is increased with the decrease of temperature and the rise HALO concentration, due to the increase of Fermi level potential and the effective channel doping concentration to be higher.

With the HALO doping concentration increases the V_{th} increases when the dimensions of these devices are reduced, owing to the higher short channel effect.

The subthreshold slope is almost the same for PD SOI MOSFET devices with and without HALO, because the HALO does not have influence on devices with the long channel length and when the temperature decreases, the subthreshold slope is lower due to influence of temperature on this parameter.

In the devices with short channel length the variation of subthreshold slope is higher due to the reduction of the depletion charge capacitance that decreases the maximum depletion depth.

It can be concluded that PD SOI MOSFET devices with HALO and operating in low temperatures present a higher advantage then the devices without HALO, because of the short channel effect reduction, that was represented by the threshold voltage increase and the subthreshold slope reduction. This work proved that the studied devices have reduced the short channel effect owing to the HALO presence as expected.

5. ACKNOWLEDGEMENTS

The author would like to thanks Carolina D. G. dos Santos from LSI EPUSP for her help support.

6. REFEFENCES

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