ANALYSIS AND MODELING OF MULTI-PHASE BUCK REGULATORS APPLIED TO MICROPROCESSORS

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ABSTRACT

A novel approach to determine L, C and respective parasitic components of a multi-phase buck converter are here described. Each one of the main stray elements associated with inductors and output capacitor are calculated by introducing new factors to describe their non-idealities. A SPICE example simulation with a multi-phase buck regulator is provided in order to attest the model validity. This methodology can be applied to any multi-phase buck converter, which must supply highly variable current loads and need to have a very low ripple output voltage.

1. INTRODUCTION

A multi-phase buck converter used in Voltage Regulator Modules (VRM), commonly supplies a microprocessor with a very low ripple output voltage, even during stringent load current transients [1] [2] [3]. Traditional methods to determine the output capacitor and inductors are only valid in cases where the load has a fixed current consumption. However, stray elements of capacitor and inductors may cause a significant influence on the ripple of the output voltage when fast load transients occur on the load current. This analysis does not impose a specific output voltage control technique during a fast load current transient, such as turning all the power switches simultaneously, in opposition to [4] [5]. In addition, the capacitance and its maximum parasites are determined initially without considering the type of capacitor used, differently from [4] [5]. Besides, other methods does not evaluate the inductances values and their stray elements.

This article shows a new technique to evaluate inductors, filter capacitor and maximum parasitic components of multi-phase buck converters in order to keep the output voltage ripple within limits accepted by the microprocessor. This analysis considers the output voltage of VRM, projecting its maximum ripple voltage according to the microprocessor manufacturer [3], which allows separating the maximum load voltage ripple in two components: the VRM voltage drift and the voltage drift caused by resistance and inductance parasites of the printed circuit board (PCB). The equation of the microprocessor voltage can be expressed as [3],

$$V_{LOAD} = (V_{VRM} \pm 20mV) - 0.00125 I_{LOAD} \quad (1)$$

The equation above shows that the load voltage is the difference between the VRM output voltage and the PCB losses, which is represented by a maximum of 1.25mΩ series impedance, corresponding to the sum of resistive and inductive PCB losses. The +/-20mV is the maximum VRM output voltage drift. As this analysis comprises only the voltage regulator module characteristics, it is not necessary to include PCB losses. Two specifications are important in order to make this analysis: the maximum load current step, called I_{MAX} and the period of the step, called Δt [3]. The load current transient has been increasing according to microprocessors evolution. Nowadays microprocessor specifications demand a step current from 0 to 100A in only 1μs [3]. Owing to its low-pass behavior, a multi-phase buck converter cannot immediately supply current through the switcher power transistors, so that the filter capacitor is the responsible for such a current. During high load transients, the output voltage control methods have little influence on its ripple.

2. ANALYSES, MODELING AND L, C AND PARASITES DETERMINATION

Figure 1 shows the simplified schematic of the power stage of a typical N-cell multi-phase buck converter, where N is the number of cells, which one comprising an inductor and respective power switches, denoted as HS (High Side) and LS (Low Side). PCB losses are not included because this analysis contains only VRM characteristics.

ESR_C and ESL_C are respectively the equivalent parasitic resistance and inductance of filter capacitor C, whereas $ESRL_N$ is the resistive loss of inductor L_N. For the example described in [3], the buck output voltage has a maximum variation of 40mV, which symmetrically divided results in a variation of +/-20mV.

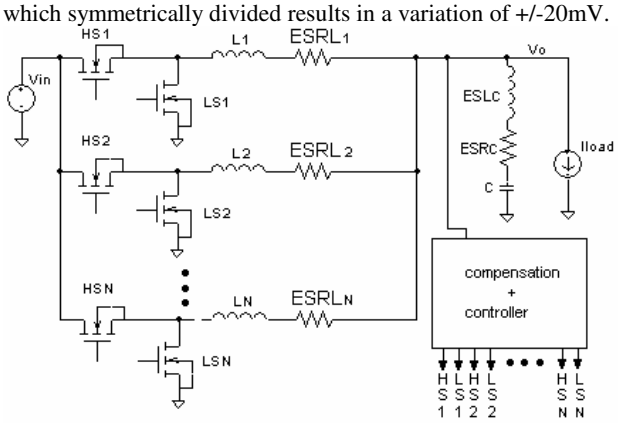

Figure 1: Typical N-cell multi-phase buck converter.

Rather than being modeled as a simple resistor, the microprocessor as a load is usually represented as a current source for transient analysis. The buck converter has a second order low-pass structure, and consequently, most of the transient load current is supplied by the filter capacitor. For this analysis, the equivalent circuit of Figure 2 is employed. It's worthy noticing that resistive losses between the DC/DC converter and microprocessor are not here considered.

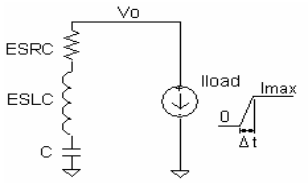

Figure 2: Modeling of buck converter output voltage during a load transient.

After the load transient, the inductor takes charge and supplies the load current. During the transient, the output voltage is reduced from its V_O to V_O^*, where V_O is the capacitor voltage for $I_{LOAD} = 0$ and V_O^* is the output voltage after a load current step. Worst-case analysis to determine values of C, ESR_C and ESL_C is now presented, based on a load current step, from 0A to its maximum value I_{MAX}, within a Δt interval,

$$\Delta V_O = V_O^* - V_O \Rightarrow \Delta V_O = (V_C^* - V_O) - ESL_C \frac{I_{MAX}}{\Delta t} - ESR_C I_{MAX} \Rightarrow$$

$$\Rightarrow \Delta V_O = \Delta V_C - (\Delta V_{ESL} + \Delta V_{ESR}) \Rightarrow \Delta V_O = \Delta V_C - \Delta V_P \quad (2)$$

where V_C^* is the voltage at the ideal capacitive component of the capacitor, after the current step, and ΔV_P is the voltage sum of resistive and inductive losses.

The factor n_C that models capacitive losses is now introduced, yielding

$$\Delta V_C = n_C \Delta V_O \quad (3) \qquad \Delta V_P = (n_C - 1)\Delta V_O \quad (4)$$

where n_C is denoted *ideality capacitive factor* and may vary from 0 to 1. If $n_C = 1$, the capacitor is ideal, without losses.

The voltage variation at the capacitive component of the model can be obtained through the charge variation on the capacitor when supplying the load current,

$$\Delta V_C = \frac{\Delta Q_C}{C} \Rightarrow \Delta V_C = \frac{-(I_{MAX} - I_{MIN})\Delta t}{2C} \therefore \Delta V_C = \frac{-I_{MAX}\Delta t}{2C} \quad (5)$$

$$\Delta V_O = \frac{-I_{MAX}\Delta t}{2C} - (n_C - 1)\Delta V_O \therefore C = \frac{I_{MAX}\Delta t}{2n_C|\Delta V_O|} \quad (6)$$

The term $|\Delta V_O|$ was used in (6) in order to make this expression simpler, because this voltage variation is negative, then the minus signal of I_{MAX} should be considered. An important outcome of this equation is the fact that the circuit performance during load current transients does not depend on the number of cells. It will be shown that N is only relevant during the capacitor recharge. Introducing another factor n_R to model the voltage drop in the resistive loss of the capacitor yields

$$\Delta V_{ESR\,C} = n_R (n_C - 1)\Delta V_O \quad (7)$$

where n_R is denoted resistive loss factor and shows the amount of capacitor losses associated with the ESR component. If such a factor is unity, the capacitor features only resistive losses. If n_R is zero, the losses are purely inductive. Reworking (2) through (7), one has

$$ESL_C = \frac{(1 - n_R)(1 - n_C)|\Delta V_O|\Delta t}{I_{MAX}} \quad (8)$$

$$ESR_C = \frac{n_R (1 - n_C)|\Delta V_O|}{I_{MAX}} \quad (9)$$

Optimal values for the capacitor, as well as for its losses, can thus be determined. The dependence of the factor n_C on the capacitor value and its losses ESR_C and ESR_L are respectively depicted in Figures 3 and 4.

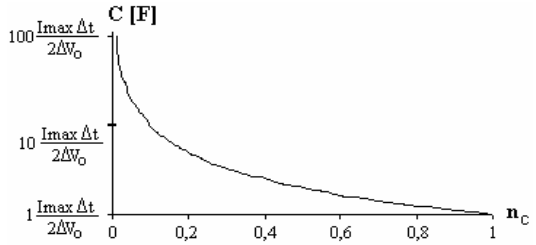

Figure 3: Output capacitance versus ideality capacitive factor (n_C).

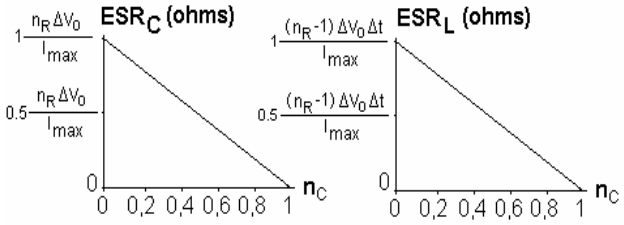

Figure 4: resistive and inductive parasites versus n_C.

These curves can be interpreted as follows. From Figure 3, if the capacitor is ideal (n_C=0), its capacitance reaches a minimum value. Choosing n_C near to ideal implies in very low losses, as shown in Figure 4. Although desirable, this can be unfeasible due to the excessive number of parallel capacitors that must be used, in order to make the ESR_C reach the calculated value. For example, if total capacitance losses are 1mΩ, the voltage at stray elements will be 100mV at I_{LOAD} = 100A, while the maximum ripple output voltage is +/-20mV [3]. Then, the typical losses for microprocessor VRM´s must be about one tenth of mΩ; then, the ripple voltage at stray elements goes to one tenth of mV, implying another tenth of mV of capacitive losses, then, the sum of these voltages continues below maximum specification. At practice, stray elements of real capacitors are about tens of mΩ, 100 times bigger the good value for the VRM. Thus, n_C must be low in order to find a practical value of parallel capacitors. Empirically, from Figures 3 and 4, n_C is adopted as 0.2, because it implies in a capacitance only 5 times bigger its minimum value, while total capacitive losses are only 20% below their maximum theoretical values. Other values for n_C can be used depending on practical factors, as price of each capacitor. Smaller capacitances imply a fewer number of capacitors in parallel, but each one of them must have a low ESR. Bigger capacitances imply cheaper capacitors, because each one of them does not need to have a very small ESR, but a bigger number of parallel capacitors are needed.

The n_R depends on the specifications of the capacitor manufacturer. An individual analysis must be made in order to find its best value. The number of capacitors in parallel must satisfy the following condition, considering all of them the same type and value.

$$N_{PC} = \frac{ESRC_U}{ESR_C} = \frac{ESLC_U}{ESL_C} = \frac{C}{C_U} \quad (10)$$

where C_U is the value of each capacitor, $ESRC_U$ and $ESLC_U$ are the resistive and inductive losses of each capacitor and N_{PC} is the number of capacitors which will be connected in parallel.

Substituting (8) and (9) into (10), n_R can be expressed as:

$$n_R = \frac{ESRC_U}{ESRC_U + \frac{ESLC_U}{\Delta t}} \quad (11)$$

After the capacitor supplies the load current, the inductor should restore it as fast as possible. Figure 5 illustrates the

equivalent schematic of the converter, including inductor resistive losses. The parasitic resistances of switchers HS and LS will not be considered in this analysis.

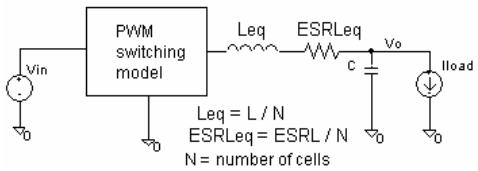

Figure 5: Equivalent model for inductor and respective losses.

To stress the importance of the parasitic resistance at converter losses, it is important to equation the circuit in two different moments: when HS is turned on, and when LS is on. It is expected that the inductance does not change its value, but it is not true to assert the same to resistive losses, as will be shown below:

2.1. HS turned on

From Figure 5, the equivalent inductor voltage when the transistor HS is turned on is:

$$V_{LEQ\_HS} = L_{EQ}\frac{I_{MAX}}{\delta T} \qquad (12)$$

where V_{LEQ_HS} is the voltage at equivalent inductance for HS on, T is the switching period and δ is the duty-cycle, which also corresponds to the ratio between the regulator output voltage and its input voltage.

Introducing a factor n_L denoted the ideality inductive factor and that represents the inductor non-ideality. Such a factor varies from 0 to unity, at which limit the inductor is assumed ideal. V_{LEQ_HS} can thus be expressed as:

$$V_{LEQ\_HS} = n_L(V_I - V_O) \quad (13)$$

$$\Delta V_{ESRLEQ\_HS} = ESRL_{EQ\_HS}I_{MAX} = (V_I - V_O)(1-n_L) \quad (14)$$

where ΔV_{ESRLEQ_HS} is the voltage at resistive parasitic equivalent of the inductor ate the moment that HS is on. Replacing (13) into (12), and from (14), L and $ESRL_{HS}$ are expressed as:

$$L = \frac{n_L(V_I - V_O)V_O N}{I_{MAX}V_I f} \qquad (15)$$

$$ESRL_{HS} = \frac{N(V_I - V_O)(1-n_L)}{I_{MAX}} \qquad (16)$$

The inductors do not need to have their ideality factors equal to unity for a large number of cells, because maximum inductive losses are proportional to N. Including HS resistive losses,

$$ESRL^*_{HS} = \frac{N(V_I - V_O)(1-n_L)}{I_{MAX}} - R_{ON\_HS} \qquad (17)$$

where R_{ON_HS} is the parasitic resistance of HS switch, when it is turned on.

2.2. LS turned on

Similarly to HS turned on, the analysis to LS turned on follows:

$$V_{LEQ\_LS} = L_{EQ}\frac{I_{MAX}}{(1-\delta)T} \quad (18)$$

$$V_{LEQ\_LS} + \Delta V_{ESRLEQ\,LS} = V_O \quad (19)$$

$$\Delta V_{ESRLEQ\_LS} = (1-n_L)V_O \quad (20)$$

$$L = \frac{n_L V_O (V_I - V_O)N}{I_{MAX}V_I f} \quad (21)$$

From (20), $ESRL_{LS}$ is expressed by:

$$ESRL_{LS} = \frac{N(1-n_L)V_O}{I_{MAX}} \quad (22)$$

Including LS resistance losses:

$$ESRL^*_{LS} = \frac{N(1-n_L)V_O}{I_{MAX}} - R_{ON\_LS} \quad (23)$$

where R_{ON_LS} is the parasitic resistance of LS switch, when it is turned on.

Thus, $ESRL_{LS}$ must be used, as this value is smaller than the one for HS. For HS turned on, the maximum inductor parasitic resistance is $\frac{V_I - V_O}{V_O}$ times LS turned on.

The factor n_L can be obtained in practice by setting $N = \frac{ESRL}{ESRL_{EQ}} = \frac{L}{L_{EQ}}$. Re-working with (22) and (21), the ideality inductor factor can be written as:

$$n_L = \frac{LV_I f}{ESRL(V_I - V_O) + LV_I f} \quad (24)$$

This factor can be obtained by iterations: initially, $n_R = 1$ is imposed. Then, L is determined. Measuring ESR_L from the physical inductor, n_L is recalculated. The new result will be a little smaller than the first inductor calculation. Taking out some turns of the inductor are enough to get the new value. After this operation, the ESR_L must be measured again. Then, a new n_L value is obtained. About 3 to 5 iterations are enough to have a good value for the ideality inductor factor.

3. APPLICATION AND SIMULATION RESULTS

Consider an output voltage of 1V, maximum transient of 100A/µs, maximum ripple of +/-20mV, input voltage of 12V, 6 cells multi-phase buck converter and ideality capacitor factor equals to 0.2. From (6), C = 12500µF. Ignoring inductive effects of capacitor implies $n_R = 1$, then, $ESR_C = 0.16m\Omega$ and $ESL_C = 0$. The factor n_L depends on the inductor construction, which depends on wire diameter, number of turns, temperature, etc. For this example will be adopted $n_L = 0.9$. Then, L = 0.165µH and $ESR_L = 6m\Omega$, ignoring HS and LS parasitic resistances.

From schematic of Figure 1, using a simple voltage feedback controller, waveforms of the multi-phase buck converter and obtained with PSPICE simulator is illustrated in Figure 6, with load varying from 0 to 100A in 1µs. The maximum output ripple is 41.15mV, 2.55% above the expected value, which is 40mV. This drift is caused by the finite response time of the compensation and the control circuit. If this time is smaller, the maximum ripple will be smaller than the calculated. The maximum current of capacitor is 91.02A, when load goes from 0 to 100A, and -88.4A when load spans from 100 to 0A. Both cases show that the capacitor current supplies about 90% of total transient load current. Using NPC capacitors, with $ESRC_U = 7m\Omega$ and $C_U = 390\mu F$ implies in 7mΩ/0.16mΩ = 44 capacitors in parallel and 390µF times 44 = 17160µF of equivalent capacitance. The final value of capacitance must be bigger than calculated, because each capacitor has a tolerance of

+/-20%. The worst-case capacitance value in this case will be 17160µF times 0.8 = 13728µF, still larger than calculated. Comparing with equations at [4] and [5], using the same input and output voltage, the same load characteristics and the same NPC capacitors, the number of parallel capacitors is 110, giving a final capacitance of 110 times 390µF = 42900µF, with ESRC of 7m/110 = 0.064mΩ, showing an unnecessary spend of PCB area, and a higher cost for using more capacitors.

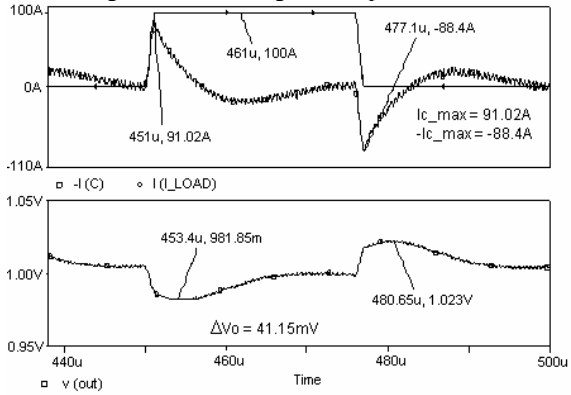

Figure 6: Load and capacitor current and output voltage waveforms versus time.

Another example of comparison, changing only the maximum transient current, from 100 to 50A, keeping other variables values, brings C = 6250µF, ESR_C = 0.32mΩ, ESL_C = 0, L = 0.33µH and ESR_L = 12mΩ. So, the number of capacitors, using the same 330µF NPC capacitors, is 22, while other techniques demands 94 parallel capacitors [4] [5], showing again an unnecessary spend of PCB area, and besides, a very high number of parallel capacitors, increasing system cost.

5. CONCLUSIONS

The present work shows a new and simple analysis to determine the minimum capacitance, the maximum inductance, and their maximum stray components to project multi-phase buck converters to VRM microprocessors, considering load current transients.

The parasitic elements of the capacitors and of inductors are the responsible for ripple in output voltage when its current load varies suddenly, because the series inductor of multi-phase buck converters cannot allow that the switchers current vary as fast as the load demands. The capacitor value must be as bigger as its stray effects, in order to compensate them. The influence of parasitic inductor elements can be minimized increasing the number of cells of the converter.

This paper describes how to calculate the maximum losses for each component, according to specifications of maximum ripple output voltage, load current behavior and VRM input and output voltages, through simple equations. The advantage of this approach is that it is not necessary to look for data sheet components at the beginning of the analysis, in opposition to other techniques, which must have the component characteristics in order to determine the parallel number of capacitors. Another advantage of this new approach is that the switching mode is not considered; then, it is not necessary to impose a specific output voltage control mode for the VRM during a load current transient. Besides, the determination of the capacitor, inductor, and their respective losses are much simpler than other techniques. Besides, this approach describes how to calculate inductor value and their maximum losses, while other techniques do not determine these components.

Supposing that the current transient is totally supplied by the capacitor, it can lead to simpler control circuits, even without current feedback, which demands good precision components to make the inductor current sensing. The control circuit used in the simulation is a simple voltage feedback, composed by frequency compensation and hysteretic comparators, proving that the output voltage keeps its value, even during transients.

The future tendency is to increase the load current transients, because of the constant evolution of microprocessors. Thus, the feedback and control methods for buck converters will be less influent in ripple output voltage during transients, making the capacitor more and more important for supplying the load current.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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