ELECTROMAGNETICS SCATTERING SIMULATIONS OF SYSTEM-ON-CHIP USING TLM-JSN WITH DIAKOPTICS TECNNIQUES

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***Abstract*— Embedded in the context of Irrigation Control Applications, a system with a wireless autonomous sensors network is been developed. As each node contains a RF transceiver, an analog and a digital circuit in the same chip, the electromagnetic compatibility analysis became essential. As a result, an EMC CAD tool was developed, using the TLM-JSN (Transmission Line Modeling - Johns Super Node) method. The diakoptics technique was applied in order to make possible big meshes simulations. This permitted a high precision EMC simulation of the SoC (System-on-Chip).**

***Index Terms*— System-on-Chip, diakoptics, Transmission-Line Matrix.**

1. INTRODUCTION

A System to control irrigation on crops has been developed by a consortium of eight institutions [1], [2]. The aim of this project is to develop a system to be used in precision agriculture, which consists of a wireless autonomous sensors network capable of evaluating soil moisture and select the optimum distribution of water.

The system is composed by a base station, field stations and nodes [3]. The field stations gather information from the nodes through a wireless link and are responsible for accurately identifying the areas of moisture deficiency and determining which nodes should act on latch solenoid valves, in order to deliver the required amount of water to the plants. The field station instructions are also sent to the nodes by a wireless link. Each node is composed by a CMOS $0.35\mu m$ [4] SoC (System on Chip), a tensiometer with a solid state pressure sensor, an actuator which controls the water flow through a solenoid valve, a solar powered power supply, a RF antenna, and embedded softwares. The SoC consists of a RISC microprocessor, memories, a RF transceiver, digital interface and A/D interface. As this chip contains an analog, a digital and a RF part together, there is a big necessity of checking electromagnetic compatibility. In this context, a CAD tool was developed to improve EMC in the chip.

The CAD is capable of calculating resultant voltage of an electric and magnetic field propagation. The software is based on TLM-JSN (Transmission Line Modeling - Johns Super Node) numerical method combined with diakoptics technique. An overview of the former is presented in next section, while the latter is explained in the third section. Finally, the simulation of SoC and its results are showed in section 4.

2. THE TLM-JSN METHOD

The Transmission Line Modeling - Johns Super Node method is a variation of time domain TLM numerical method [5], which consists of discretizing the space in a Cartesian mesh and representing each node as a junction of transmission lines. Impulses of incident and reflected voltages are propagated in the mesh representing electromagnetic waves. This process is described as a function of steady-state incident and reflected voltage waves at the nodes or boundaries, V^i and V^r, respectively.

A state equation formulation is used in TLM-JSN to relate the incident and the reflected voltages. In the JSN method, the problem is divided into external and internal domains. This allows the creation of an interconnection of macrocells, which is the basis of diakoptics techniques (explained in Section 3). The TLM-JSN algorithm may be expressed by the interactive calculation of:

$$[_{in}V]^r_k = \left[T^t\right] . [_{ex}V]^i_k + [C] . [S] . [_{in}V]^i_{k-1} \quad (1)$$

$$[_{ex}V]^i_k = [T] . [S] . [_{in}V]^i_k \quad (2)$$

where $[S]$ is the scattering matrix that refers to the mesh nodes, $[C]$ is the connection matrix that describes the network's topology and $[T]$ is the transmission matrix that represents the relation between external and internal domains. In (1) and (2), k and $k+1$ indicate the discretized time step in which the steady-state incident and reflected voltages are calculated. A detailed description of TLM-JSN method may be seen in [6], [7].

3. THE DIAKOPTIC TECHNIQUE

The simulation of structures like SoC is very challenging because of their complexity, which forces the use of a big mesh to represent them. If all the SoC was simulated as a single block, the matrices would be too big, which would result in a huge computational effort or even make the simulation impossible. This problem makes the diakoptics technique very attractive. The diakoptics technique (from Greek, *dia* = system + *koptic* = cut) consists in dividing large structures in sub-structures, which are simulated apart and then reconnected in order to find a solution to large scale problems. This technique has been widely applied with frequency methods. In 1981, however, a proposal for application of this technique in time

domain TLM was presented by P. B. Johns e Akhtarzad [8], [9].

The diakoptics are applied with TLM-JSN method based on equations (1) and (2). As in expression used in [8], [9], these equations also represent the influence of mesh inner behavior on internal voltages $\left([C].[S].[_{in}V]^i_{k-1}\right)$, but with the addition of external sources $\left([T^t].[_{ex}V]^i_k\right)$.

Each subdivision is considered as an additional parallel simulation and their outputs in time step k become inputs of other blocks in time step $k+1$. This is made through interconnection matrices responsible for changing information among marginal branches of neighbor blocks. These auxiliary matrices are just pieces of $[T]$ matrix of the block, corresponding to upper, bottom, left and right branches separately.

The system solution is, therefore, obtained by parallel processing of smaller dimension systems, which reduces the computational effort.

4. SoC Simulation and Results

As mentioned before, the System-on-Chip analyzed with this EMC CAD tool has an RF part. Thus, an important preoccupation in this SoC project was the interference that it could cause on analog and digital parts.

The RF transceiver is showed in Fig. 1, with an identification of its main components. This transceiver is enclosed with metal paths in order to create an electromagnetic protection for remain of the circuit. The RF transceiver operates in the ISM band ($915 - 927.75$ MHz) with OOK modulation, 50 KHz transmission channel and Half-Duplex mode. A 16 MHz external crystal-oscillator is the only reference frequency for the entire SoC.

In the case of SoC simulation, the chip was discretized in two regular meshes: the TLM method used 486×486 nodes and the diakoptics used 18×18 blocks, as it is illustrated in Fig. 2. The area of SoC is square shaped, with side of $6mm$, thus we obtained the dimensions of $\Delta x = \Delta y = \Delta \ell = 12.3\mu m$ and the corresponding time step $\Delta t = 0.0582ps$. Since the output of the antenna is the sixth PAD, we chose an excitation point near the end of it. The simulation consisted on applying a 3.8V- amplitude gaussian voltage pulse with a DC value of 1.2V at the excitation point, in order to analyze how it would propagate. Therefore, the simulation starts with a peak of 5V applied on the excitation node and the value of this external excitation is reduced on next time steps, creating a Gaussian pulse centered in $t = 0$s. This excitation was chosen because the supply voltage used in the RF transceptor is 1.2V and the maximum voltage peak produced due to decoupling inductors is 5V. Besides, the maximum gate voltage supported by this technology is 5V.

The System-on-Chip developed in this project contains 4 metal layers, which were simulated separately. Fig. 3 presents the simulation result of the first metal layer in 3 different time steps: 50, 100, 150 and 200, which correspond to $t_1 = 2.91ps$, $t_2 = 5.82ps$, $t_3 = 8.73ps$ and $t_4 = 11.64ps$, respectively.

Although the simulation presented voltages higher than 0.1V, this value was chosen as the limit of color scale, which means every voltage equal or greater than this was plotted in white. The figure was made like this in order to make possible an observation of wave propagation, once most of the points have small voltage values. Looking to color scale, it is also possible to observe that simulation gives the absolute voltage values. This is due to the way used to calculate the resultant voltage in each node. As a result of TLM-JSN calculations, the voltage in each branch of a node is obtained. Using the energy conservation principle in TLM, the total voltage in a node is given by:

$$V_{node} = \sqrt{V_{b1}^2 + V_{b2}^2 + V_{b3}^2 + V_{b4}^2} \tag{3}$$

where V_{bi} is the internal incident voltage in the ith branch of that node.

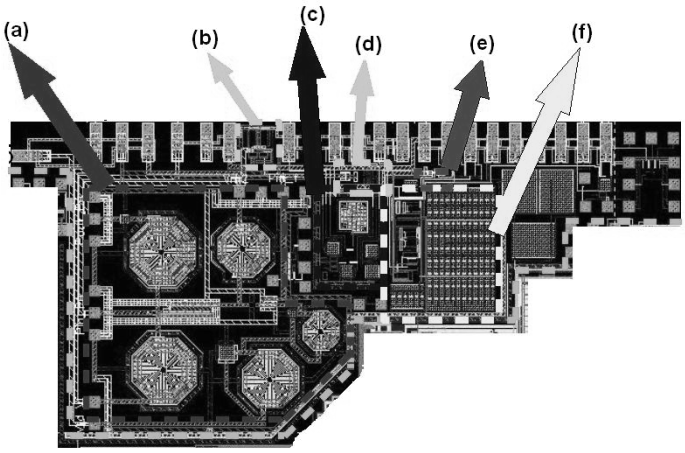

Fig. 1. Transceiver characteristic: (a) Power Amplifier (PA), (b) Antenna switch, (c) Low Noise Amplifier (LNA), (d) TX switch, (e) Demodulator and (f) Frequency synchronizer.

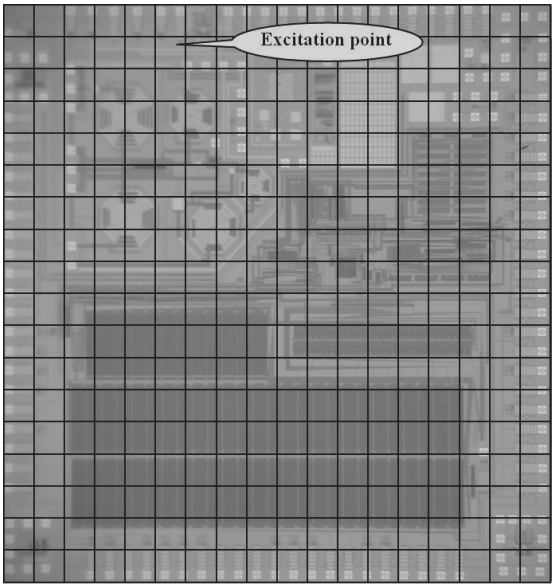

Fig. 2. Diakoptics discretization of SoC, with a regular mesh of 18×18 blocks. Each block corresponds to 27×27 nodes, resulting in a total TLM mesh of 486×486 nodes.

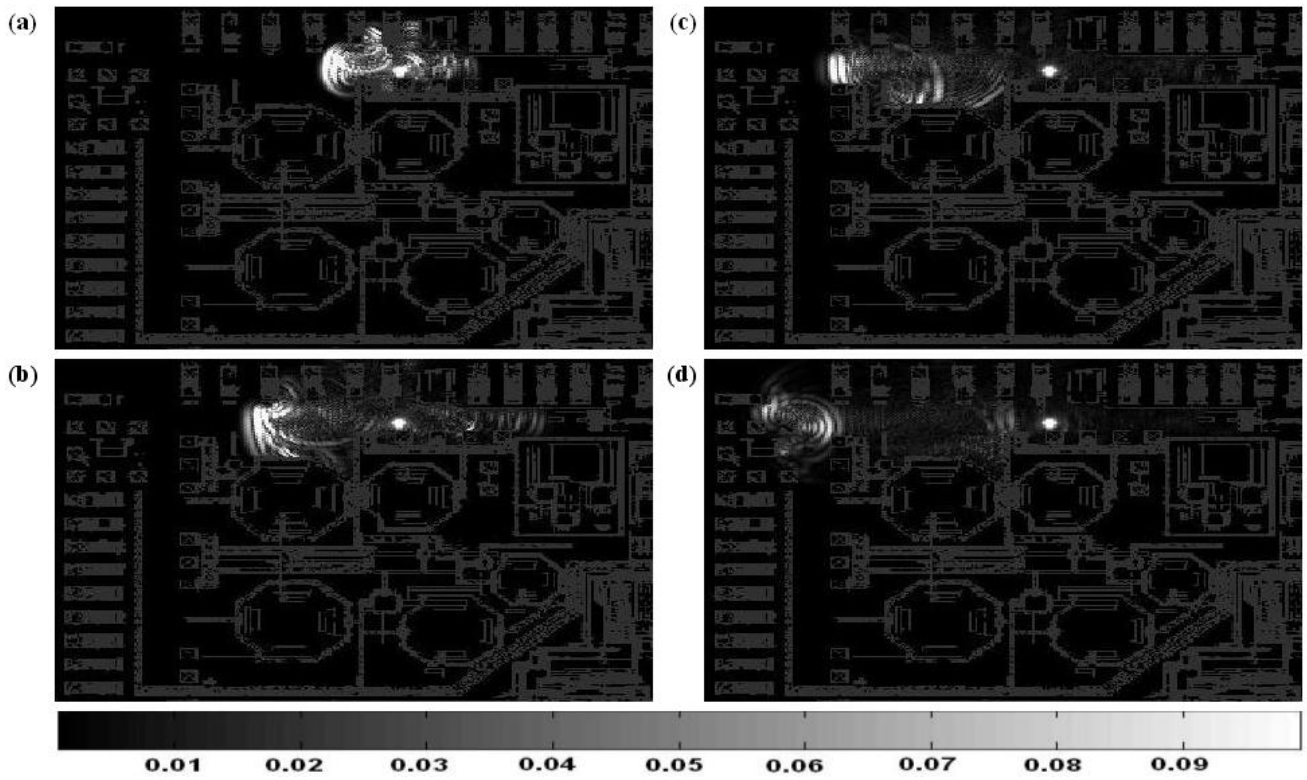

Fig. 3. Electromagnetic propagation with (a) 50, (b) 100, (c) 150 and (d) 200 times steps (respectively,$t_1 = 2.91ps$, $t_2 = 5.82ps$, $t_3 = 8.73ps$ and $t_4 = 11.64ps$) using Gaussian pulse.

Observing the numerical results, we can see that the maximum voltage value obtained was 5.4613V, in a node near the excitation point ($\Delta x = 61.1\mu m, \Delta y = 0$). This value was achieved on 20^{th} time step. Although it was bigger than the voltage usually supported by this technology, it occurred during a very short interval. Besides, the excitation pulse was a worst case test. Thus, the result of this simulation was very satisfactory and can be used as part of the SoC system validation.

5. Conclusion

This work presents the result of a combination of TLM-JSN method with the diakoptics technique, which allowed the reduction of computational efforts and consequently made the simulation of big structures possible. The CAD tool, developed to improve EMC in the SoC, is an important step on chip electromagnetic simulations. The CAD provided a cartographic analysis of the RF field distribution along the chip, allowing an estimation of RF interference at various chip locations. That feature may help on placement strategies since it indicates areas which are more exposed to RF interference. Presently, this CAD tool makes 2D simulations only. Simulations have been carried out up to now on single separate metal layers. The combined simulation of all metal layers is under development.

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