CHARACTERIZATION OF A ROM TEST STRUCTURE DESIGNED FOR A SOC FOR IRRIGATION CONTROL

José Edil G. de Medeiros, Gilmar S. Beserra, Helder H. Guimarães, Adson F. da Rocha, José C. da Costa

Universidade de Brasília
Faculdade de Tecnologia – Departamento de Engenharia Elétrica
{jose.edil,gilmar.beserra,hhguimaraes}@gmail.com, {adson,camargo}@unb.br

ABSTRACT

In this work, a MOS ROM test structure was designed and tested in order to validate the chosen architecture for a 2-Kbyte ROM that will integrate a RISC16 microprocessor. The purpose of the ROM is to store system initialization routines for a System on Chip (SoC) for irrigation control on crops. A full version of the complete SoC including isolated modules for test was fabricated using CMOS 0.35μm technology. The ROM tests were performed successfully and the results corresponded to the technical specifications.

1. INTRODUCTION

Precision farming acknowledges that conditions for agricultural production – as determined by soil resources, weather, and previous management – vary across space and over time. Given this inherent variability, management decisions should be specific to time and place rather than rigidly scheduled and uniform. In order to help this decision-making, a system to control irrigation on crops is being developed [1]. The system is composed by a base station, field stations and nodes.

The field stations gather information from the nodes through a wireless link and transmit them to the base station, which accurately identifies areas of moisture deficiency and displays them to the user, helping to program the system behavior. Each node is composed by a SoC, a tensiometer with a solid state pressure sensor, an actuator which controls the water flow, a solenoid valve, a solar powered power supply, a RF antenna, and embedded softwares. The SoC consists of a RISC microprocessor, memories, a RF transceiver, digital and A/D interfaces. Because it is composed by several modules, this project presents challenges like Electromagnetic Compatibility (EMC) and Electromagnetic Interference (EMI) [2].

The system has a 2 KB ROM to store setup routines. A 6 KB SRAM memory [3] will be used to store the application softwares. The storage capacity was defined according to the minimal functions needed by the application programs.

A hardware and software co-design approach is adopted in the SoC development. The application software that is being implemented will be used to read soil-moisture-sensors data and control the irrigation equipment. The system will automatically collect, process, record and transmit the soil data to the field station. Besides the application software, a boot program was designed and stored in the SoC's ROM prototype [4]. A communication protocol was developed to allow the data transfer between the interfaces and the SoC [5].

This paper presents the characterization of a test structure that was implemented to validate the ROM architecture. The paper outlines as follows: Section 2 describes the design methodology, Section 3 presents the implementation of the ROM architecture, Section 4 shows the test performed in the fabricated chip, Section 5 shows the results and finally section 6 presents the conclusions.

2. DESIGN METHODOLOGY

A full-custom design methodology was adopted using both top-down and bottom-up approaches. The ROM module was designed using test points to improve the observability of the internal signals. An isolated test structure composed by a 4-word ROM was also sent with internal pads to test the chosen architecture. The chip was fabricated using Austria Microsystems 0.35 μm CMOS technology with 4 metal and 2 poly layers [6].

3. ROM DESIGN AND IMPLEMENTATION

A 2 KB CMOS ROM was specified to integrate the microprocessor in order to store system initialization routines that will manage the hardware structure for communication with the other modules.

In this first prototype, a 256-word ROM (512 Bytes) was enough to store the boot routine designed to perform the tests. The cells were implemented with only one transistor per bit of storage and arranged as a NOR array, as suggested in [7]. Figure 1 shows the diagram of the ROM including a decoder and a parallel-serial converter to minimize the number of pads. When L_S=1, the load operation is performed, and data presented in the inputs are stored in the flip-flops. When L_S=0, the stored data are shifted out every rising edge. The first output value corresponds to the less significant bit (LSB).

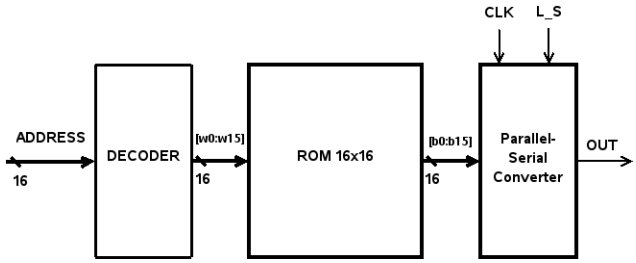

Figure 1. 512-Byte ROM diagram.

ROMs are usually tested using specific techniques, such as BIST (Built-In Self Test). In this case, due to its simplicity, the circuit was tested using another approach. A small test structure named TESTE_MATRIZ (Figure 2) was included on the chip with internal pads. It is similar to the 512-Byte ROM, but has only 4 words (8 Bytes) arranged in two columns. Dynamic pull-up circuits are selected according to the column in which data will be read, otherwise they remain disabled. Since there are only two rows (W0 and W1) and two columns (col0 and col1), a single input was used to enable each one. In other words, because each row and column must be selected at a time, w1 = not (w0) and col1 = not (col0). Each address stores a 16-bit word (2 Bytes), and because of that a parallel-serial converter was included in the circuit output.

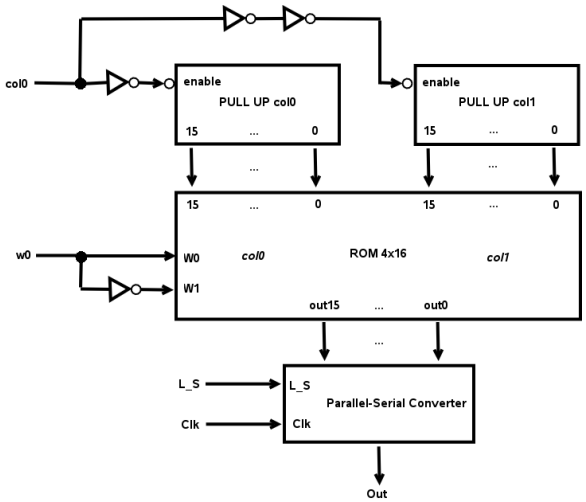

Figure 2. TESTE_MATRIZ schematic.

Table 1 shows the data stored in each one of the four addresses. By selecting w0 and col0, it is possible to read the output by configuring the converter to load the word and shift each bit during 16 clock cycles.

w0	col0	Output (hexadecimal)	Output (binary)
1	1	0123	0000 0001 0010 0011
1	0	4567	0100 0101 0110 0111
0	1	89AB	1000 1001 1010 1011
0	0	CDEF	1100 1101 1110 1111

Table 1. Addresses and stored data.

3.1. Simulation

Spectre [8] simulations were performed to read the stored data in the four available addresses. As an example, Figure 3 shows the waveforms of the data reading out from the address "11" (w0=1 and col0=1). It is important to notice that the first output corresponds to the less significant bit, and that this output is already available with L_S=1. The other outputs are obtained in the next 15 clock cycles by doing L_S=0 (shift operation).

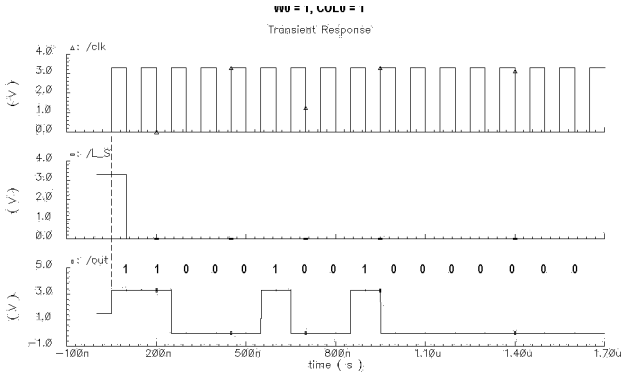

Figure 3. TESTE_MATRIZ simulation.

3.2. Layout

After simulation, the layout of the structure TESTE_MATRIZ was made using Virtuoso environment [8] and all the verifications were performed. Figure 4 shows this structure near the left top corner of the fabricated chip.

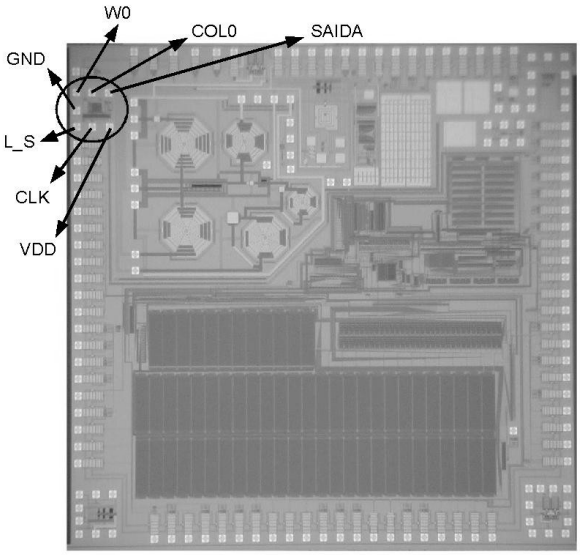

Figure 4. SoC layout showing TESTE_MATRIZ location.

4. TEST AND CHARACTERIZATION

A Keithley 2400 source-meter was used as power supply. Its capacity to measure the current of the device under test (DUT) allows to perform other tests like IDDQ (quiescent state supply current test). An Agilent 1670G programmable logic analyzer was also used. It has 136 channels that operate in several frequencies up to 150 MHz. Its IO ports operate with a 5V power supply. Figure 5 shows the measurement setup.

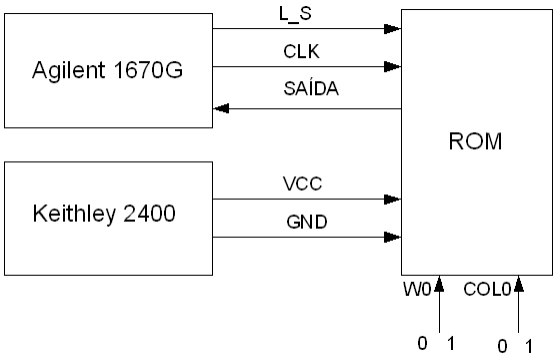

Figure 5. Test diagram.

The access to the structure inside the chip was made using a semi-automatic probe station as can be seen in Figure 6.

Since the frequency operation is low (20 and 40 MHz), special procedures like shielding and the use of RF station were not necessary. The probe station and all the equipment were properly grounded.

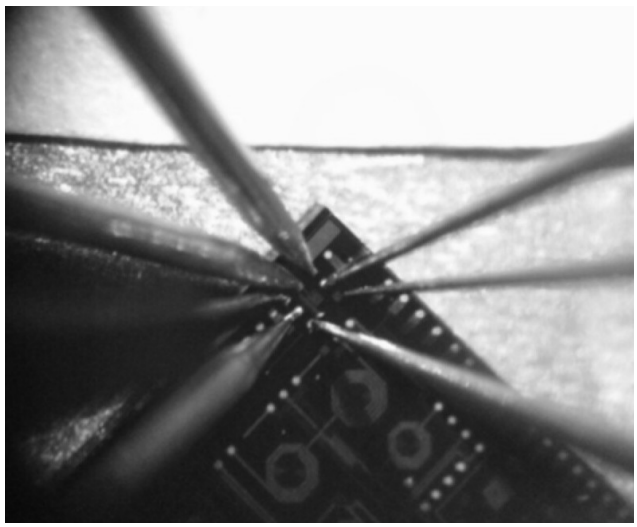

Figure 6. Probes in place for test.

5. RESULTS

The results obtained in the logic analyzer with w0=1 and col1=1 are shown in Figure 7. It is possible to notice that the waveforms are similar to the simulation, shown in the Figure 3.

The tests were performed in two different frequencies: 20 MHz and 40 MHz. Since the RISC16 microprocessor frequency operation is defined as 16 MHz, the designed ROM memory was succesfully validated. The other circuits that were designed and implemented by our team - such as the parallel-serial converter and the input and output buffers - were used in the test structure and were also validated.

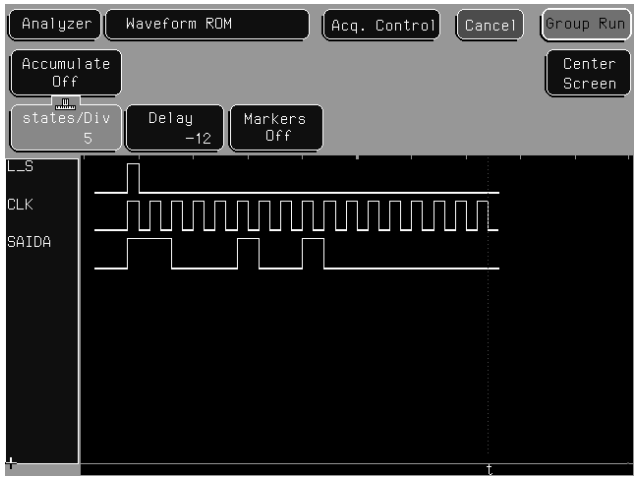

Figure 7. Test results.

Since the circuit was working properly with 5V, it was also possible to validate the voltage range of the 0.35um CMOS AMS technology (0 - 3.3V up to 5V).

6. CONCLUSION

A SoC is being designed for application in precision farming. The SoC contains a microprocessor, memories, digital and analog interfaces, and a RF transceiver. A ROM memory was designed for this SoC, validated by simulation and sent for prototyping. A small ROM test structure was sent to validate the chosen ROM architecture. This structure was tested and the measurements obtained were similar to those showed in the simulations. A full version of the SoC will be implemented taking into account the results from the previous prototyped blocks characterization that are still being tested.

7. ACKNOWLEDGEMENTS

The authors would like to acknowledge CAPES, CNPq and PADCT/Millenium Institute (Brazilian government agencies) for financial support.

8. REFERENCES

[1] “O Livro Branco do Sistema de Controle de Irrigação”, SCI, Instituto do Milenio SCMN, Julho 2003, unpublished (in Portuguese).

[2] J.C. da Costa *et al*, “CMOS SoC for Irrigation Control”, Proceedings of IEEE International SoC Conference, Washington, USA, pp. 51-54, 2005.

[3] G.S. Beserra, “Projeto de Estruturas de Armazenamento Digital em um SoC para Controle de Irrigação”, Master Thesis in Electrical Engineering, University of Brasília, Brazil, 2004 (in Portuguese).

[4] A.L. da Silva, “Desenvolvimento de Softwares para a Comunicação de Sistemas Integrados em Chip (SoC) Aplicados a Sensores para Controle de Irrigação”, Final Project in Electrical Engineering, University of Brasília, Brazil, 2005 (in Portuguese).

[5] G.L. Ishihara, “Protocolo de Comunicação para uma Rede de Sensores sem Fio: Teoria e Implementação em SoC”, Master Thesis in Electrical Engineering, University of Brasília, Brazil, 2006 (in Portuguese).

[6] AMS (Austria Microsystems) 0.35 um CMOS, Model C35B4C3, 4 metal levels, 2 poly levels, 3.3V-5V power supply (http://www.austriamicrosystems.com/).

[7] Weste, N. H. E., and K. Eshraghian, *Principles of CMOS VLSI Design – A Systems Perspective*, 2nd ed., Addison-Wesley, 1992.

[8] Cadence Design System Inc. Version 5.1.4.1 (http://www.cadence.com).