Reconfigurable CORDIC Based Digital Modulator

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ABSTRACT

This paper describes the design of a reconfigurable digital modulator to be integrated in the terrestrial platforms of Brazilian Data Collecting System. The modulator proposed is based on the CORDIC algorithm and has several configurable parameters, such as carrier frequency, modulation type (AM, PM or FM) and modulation index. The modulator model was coded in VHDL and then prototyped and validated in FPGA. The experimental results summarized in this paper shows the modulator signals in the output of the system.

1 INTRODUCTION

The Brazilian Data Collection System (BDCS) [1] is constituted by satellites, receiving stations and Data Collection Platforms (DCP). The DCPs are formed by sensors and transmitters and are scattered along the brazilian territory collecting mainly meteorological and hydrological information. They transmit the data for the satellites that relay the messages for the earth station. The designed modulator will replace old transmitters technologies, improving its performance and flexibility.

The Coordinate Rotation Digital Computer (CORDIC) [2], [3] is a computing algorithm widely used in digital signal processing and in software defined radio (SDR) applications. It is based in coordinate vector rotation and can be easily implemented using only adding and shifting operator. The proposed modulator uses CORDIC for vector rotation and signal generation in addition to a controlled phase accumulator[1], [4].

After this introduction, the BDCS is detailed in section 2. Then, in section 3, the CORDIC algorithm is explained. The modulator design is covered in sections 4 and 5, and before conclusion, the results are presented in sections 7 and 8.

2 BDCS - DCPs AND SATELLITES

The Data Collecting System [1], of Space Research National Institute (SRNI), is composed for approximately 600 Data Collecting Platforms distributed over the country, 3 satellites (SCD-1, SCD-2 and CBERS2), 2 receiving stations and a Data Collecting Mission Center, located in Cachoeira Paulista SP. The meteorological data captured for the sensors of DCPs are transmitted for the satellites. The transponder embedded on the satellites only relay the messages for the receiving ground stations. From the reception stations, the data are sent to the Mission Center to be processed and distributed for the internet users. This is illustrated in Figure 01.

Figure 1: Brazilian Data Collection System

The modulation modules are part of both the DCPs transmitter and the satellite's transponder. The modulator designed will be part of a new transmitter of DCPs developed in FPGA, since the required volume is not enough for ASIC production. The DCPs transmitters, as standard, modulate the information in PSK with modulation index of 60°/V, but other services can demand others modulation modes with different modulation indexes . This design takes care of these perspectives offering flexible configuration, the current transmitters do not offer this advantage.

3 CORDIC ROTATION MODE

CORDIC is an iterative method that can carry out several signal tasks from the vector rotation. The algorithm owns two forms: Rotation Mode (RM) and Vectoring Mode (VM) [1], [3]. The CORDIC equations are:

$$X_{i+1} = X_i - d_i \cdot 2^{-i} \cdot Y_i,$$

$$Y_{i+1} = Y_i + d_i \cdot 2^{-i} \cdot X_i,$$

$$\theta_{i+1} = \theta_i - d_i \cdot arctg(2^{-i});$$

where X_i, Y_i and θ_i are the inputs and the direction of rotations d_i are chosen by:

$$d_i = sign(\theta_i) \text{ in rotation mode,}$$

$$d_i = -sign(Y_i) \text{ in vectoring mode.}$$

A functional block of CORDIC Rotation Mode is illustrated in figure 2, where K is a constant gain factor of iterations. From the Rotation Mode a controlled oscillator can be obtained. The reconfigurable modulator is based on this oscillator, whose phase and amplitude can be controlled by changing the X_{in} and/or θ_{in} inputs.

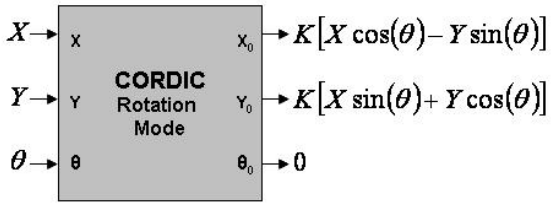

Figure 2: CORDIC Rotation Mode

4 MODULATOR - REFERENCE MODEL

Before the design in VHDL, the modulator was coded in a high level language, the C language. The design serves as a reference model to the final design. The reference model is used for functional verification of the VHDL model. The same test vectors are used in both the reference and VHDL models. The output signals must be equivalent in the two cases.

In Fig. 3 the flow is showing an action sequence of a modulation designed in C language. A text file with the modulating signal is read by the C software. The program outputs a text file with the modulated signal that will serve as a reference for the outputs of VHDL design.

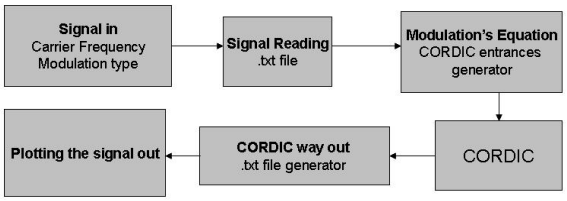

Figure 3: C language sequence of a reference model

5 IP - CORE MODULATOR

The design of the Modulator (Fig.4) in VHDL is divided in functional blocks: CORDIC, adder, register and Mux (to select the modulation type and index). All blocks were designed as generic [5], that is, with N-bits. The CORDIC block was designed

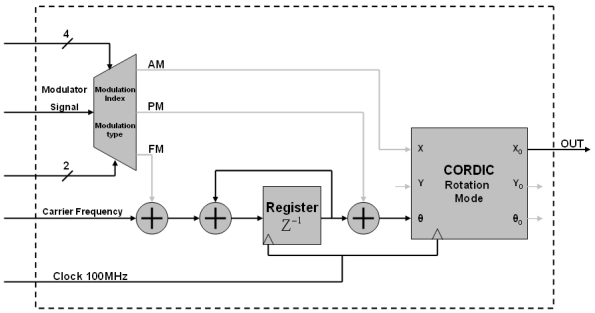

Figure 4: Digital Modulator (Block Diagram)

pipelined [3](Fig.5) with registers between each iteration, making it possible the sample frequency increase. The number of iterations of CORDIC also can be configured.

The IP-Core Modulator has 5 inputs: Modulation Index Selector, Modulation Type Selector, Carrier Frequency Value, Clock and Modulation Signal Input. The Modulation Index Selector is a 4-bit number which select a divide constant between 1 and 16. The Modulation Type Selector is a 2-bit number which chooses a modulation type (AM, PM, FM and Carrier). If carrier is to be chosen, only the carrier signal is observed in the output. Carrier Frequency is an N-bits number which is present in the all phase accumulators. The Clock is a 1-bit input, control of the sample of circuit. The modulation signal is an N-bits input for the base-band signal.

6 EXPERIMENTAL MODEL

To implement the modulator, an experimental model was set up using a development kit based on an Altera FPGA Cyclone II EP2C70F672C6N, a signal generator and a spectrum analyzer (Fig.6). During the experiments, the carrier frequency was fixed in 10 MHz, the internal clock used was of 100

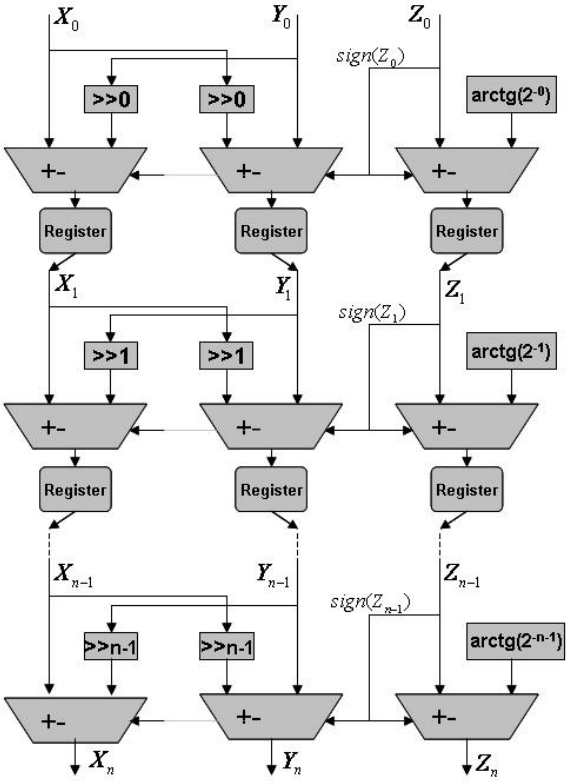

Figure 5: CORDIC pipelined structure

MHz (sample rate 100 MS/s) and the signals bit-width was 12 bits.

For the selection of the modulation index and type, a dip switch available in development kit was used in order to select the index modulation, a 4-bit number is selected in four switches. To select the type modulation, a 2-bit number is selected in two switches. This kit contain DAC and ADC converters, used in the input and output signal of modulator.

The VHDL design as well as the FPGA configuration were done in the Altera Quartus environment[5].

7 MEASURING TESTS RESULTS

The result of measuring tests presented in next figures was acquired of a spectrum analyzer with carrier signal frequency of 10MHz and base-band signal frequency 100 KHz, and every modulation types.

The Fig. 7 show two PM modulated signals with two different indexes modulation (side bands attenuates 20dB), the first when the word "1111" (divide constant = 1) is selected in dip switch and the second when the word "0000" (divide constant = 16) is selected. The AM output signal is illustrated in figure 8, it shows a spectrum of the modulator output signal.

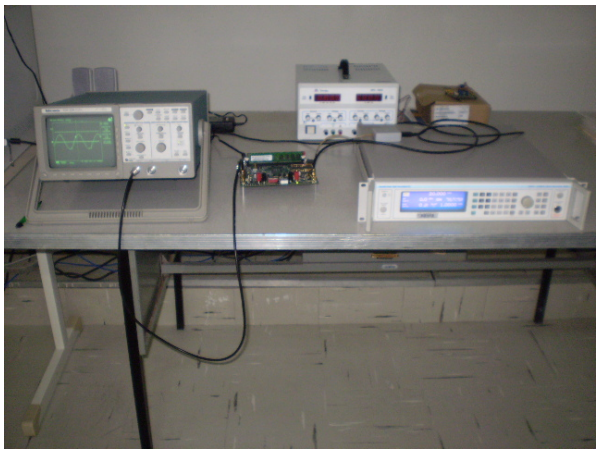

Figure 6: Experimental Model of Modulator

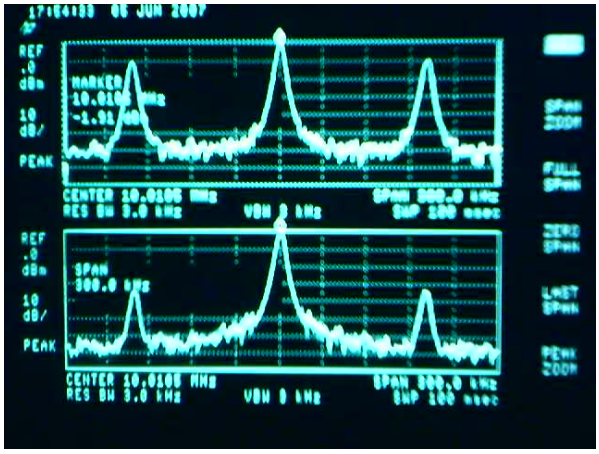

Figure 7: Spectrum of the modulator output signal when PM is selected with two different index modulations.

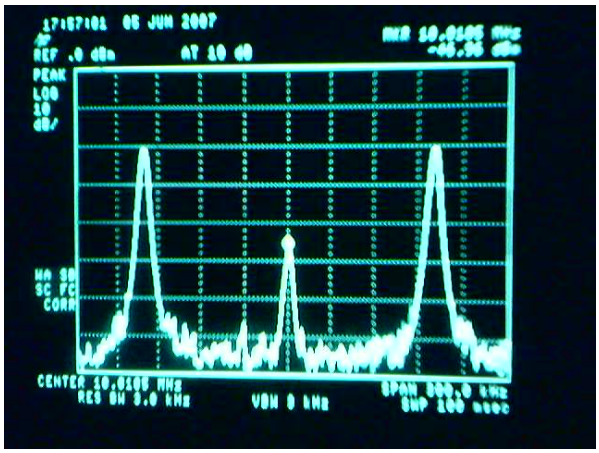

Figure 8: Spectrum of the modulator output signal when the AM modulation is selected.

PSK modulation is used in the DCPs that can be obtained using the designed modulator, in this case the input is a binary signal as well as in the FSK and ASK modulations.

The FPGA used resources are shown in Tab.1, from which we can notice that the proposed design only consumed 2.4% of total logic elements and 9.5% of a total pins of FPGA, therefore a small FPGA can be used in the final circuit or more functionalities can be increased to the design, using the same device.

	Available	Used
Total Pins	422	40 (9.5 %)
Memory Bits	1152K	426K (27 %)
Multiplier	300	26 (8.7 %)
Logic Elements	68416	1636 (2.4 %)

Table 1: FPGA EP2C70 used resources.

8 CONCLUSIONS

CORDIC is a powerful tool for the design of digital domain circuits. The realized CORDIC based modulator has as main advantage the versatility and adaptability in the communication systems. This design is a functional block, thus, it can be used in others systems beyond the DCPs transmitter and satellite's transponder. The measuring tests results shows the efficiency and reconfigurability of the designed modulator.

A serial (RS-232) interface is being designed on the UART block of the NIOS II, a configurable processor of ALTERA. This will be interface between the sensors of DCPs and the digital modulator.

9 ACKNOWLEDGEMENTS

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