HARMONIC DISTORTION COMPARISON BETWEEN CIRCULAR GATE AND CONVENTIONAL SOI nMOSFET USING 0.13 µm PARTIALLY-DEPLETED SOI CMOS TECHNOLOGY

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ABSTRACT

The Harmonic Distortion or Linearity is an important merit figure for low-power, low-voltage analog integrated circuits applications. This paper studies the Harmonic Distortion in Circular Gate SOI nMOSFET, using 0.13 µm Partially-Depleted SOI CMOS technology for analog applications. The drain/source asymmetric effects are considered in terms of the drain current as a function of the gate and of the drain voltage. The circular gate SOI nMOSFET Harmonic Distortion comparisons with the conventional (rectangular gate) partially-depleted SOI nMOSFET are performed, regarding the same effective channel length and width. This paper is based on experimental results. The Integral Function Method (IFM) is used to determine the total harmonic distortion (THD) and the third order harmonic distortion (HD3) in order to perform this work. It is observed that circular gate presents improved harmonic distortion as compared with the rectangular gate SOI nMOSFETs, for the same effective channel length and width, operating in the saturation region.

1. INTRODUCTION

The harmonic distortion is an important merit figure for low-power low-voltage analog integrated circuit applications, as for the Operational Transconductance Amplifiers (OTAs), one of the main basic analog built blocks. When a signal is applied to the transistor gate, the harmonic distortion occurs due to the I_{DS}-V_{GS} non-linearity characteristic in the saturation region, as indicated in figure 1.

To measure the harmonic distortion, it is necessary to apply a signal in the transistor gate (V_{GS}) and to measure the output signal. The device linearity can be obtained considering an input sinusoidal signal given by the equation (1).

$$V_{GS} = V_0 + V_a \sin(\omega t) \qquad (1)$$

where V_0 is the DC gate to the source bias and V_a is the maximum amplitude value of the sinusoidal signal.

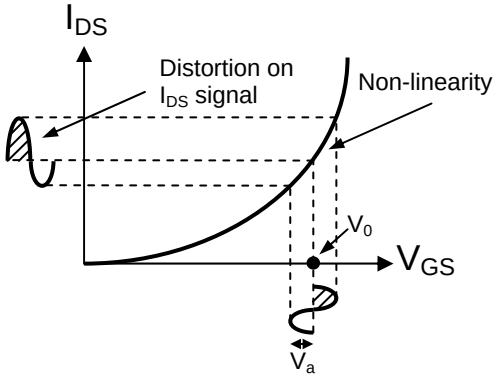

Figure 1 – Drain current distortion caused by non-linearity in I_{DS} versus V_{GS} curve.

The Total Harmonic Distortion (THD) of a signal is defined as a sum of all harmonic frequency powers above the fundamental one over the fundamental frequency power and it is usually expressed in dB [equation (2)] [2].

$$\mathrm{THD} = \frac{\sum \mathrm{harmonic\_powers}}{\mathrm{fundamental\_freq.\_power}} = \frac{\mathrm{P2} + \mathrm{P3} + \mathrm{P4} + \ldots + \mathrm{Pn}}{\mathrm{P1}} \qquad (2)$$

where P1 is the power level of the fundamental frequency harmonic and P2, P3, P4 and Pn are the power levels of the harmonic components presented in the output signal.

The Integral Function Method (IFM) is used to determine the total and the third order harmonic distortions [1, 2]. This method uses only the device DC electrical characteristic (I_{DS}-V_{GS}), instead of Fourier-based methods, which require complicated AC characterization.

New devices [Graded-Channel (GC), Double Gate SOI nMOSFEI, etc] and new techniques (circuit layouts that degrade the die area and the parasitic capacitances) can be used to improve harmonic distortion [3-5]. Another possibility is to study the influence of the gate

geometrical form in Linearity, for the same technology. The circular gate transistor (CGT) [6], presented in figure 2, is an option.

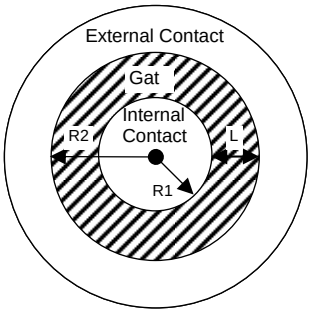

Figure 2 - Circular gate SOI nMOSFET layout.

In figure 2, L is the channel length (= R2 – R1), and R1 and R2 are internal and external radii of the channel. Note that CGT presents drain and source asymmetric dimensions. The internal contact can operate either as a drain or as a source. This device can be biased in two different ways: the internal and the external drain configurations.

The geometric factor (f_r) of the conventional (rectangular gate) transistor and the CGT is given by the equation (3) [7].

$$f_r = \left(\frac{W}{L}\right)_{Rectangular} = \left[\frac{2\pi}{\ln\left(R2/R1\right)}\right]_{Circular} \qquad (3)$$

The objective of this paper is to study the Total Harmonic Distortion and the Third Order Harmonic Distortion behaviors in the circular gate SOI nMOSFETs taking into account the drain/source asymmetric effects, base on experimental results. The comparisons between the conventional and the circular gates SOI nMOSFETs are also performed, considering the same effective channel length and width.

2. PROCESS AND ELECTRICAL CHARACTERISTICS

The devices were fabricated at IMEC, Belgium, using the 0.13 μm Partially-Depleted SOI CMOS technology. The technologic parameters of the SOI nMOSFETs are: t_{oxf} = 2.5 nm (gate oxide thickness), t_{oxb} = 400 nm (burred oxide thickness), t_{si} = 100 nm (silicon thickness), N_A = $5.5x10^{17}$ cm^{-3} (channel concentration), $N_{Drain/Source}$ = $1x10^{20}$ cm^{-3} (Drain/Source concentration). The CGT dimensions are L = 1 μm (channel length) and W = 100 μm (the average channel width). In order to obtain W/L = 100, using the expression (3), R1 and R2 values of the circular gate transistor are 15.5 μm and 16.5 μm, respectively. The conventional transistor dimensions are L = 1 μm and W = 10 μm, resulting W/L = 10.

The CGT and the conventional threshold voltages (V_{TH}) are extracted by using the second derivative method and their values are 0.31 V and 0.33 V, respectively.

The figure 3 presents experimental normalized drain current [I_{DS}/(W/L)] as a function of drain to source voltage (V_{DS}) of CGT with the internal and external drain configurations and the conventional SOI nMOSFETs, for different gate to source voltages (V_{GS}). The normalized drain current [I_{DS}/(W/L)] is used to eliminate the dimensions effects in linearity comparative study between the CGT and the rectangular gate SOI nMOSFETs.

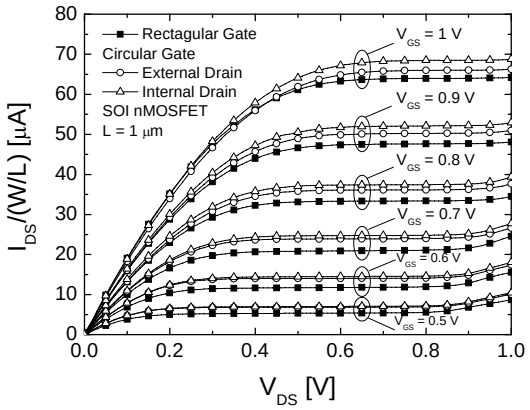

Figure 3 – I_{DS}/(W/L) versus V_{DS} of rectangular and circular gate SOI nMOSFETs.

The drain current of the CGT operating with the internal drain configuration is higher than operating with the external drain and the conventional SOI nMOSFET, due to the pinch-off point of the CGT with the internal drain configuration is more distant from the drain than the external drain configuration [6] and consequently the effective channel length of the CGT with the internal drain configuration is smaller than the external drain configuration, resulting in higher drain current. Besides, as the gate voltage increases, bigger are the drain current differences between the internal and the external configurations and also the conventional device.

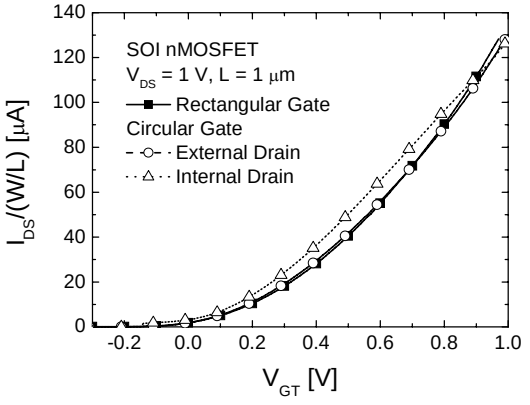

Figure 4 – $I_{DS}/(W/L)$ versus V_{GT} of rectangular and circular gate SOI nMOSFETs.

To eliminate the threshold voltage differences between the CGT and the conventional one, figure 4 is plotted normalized drain current as a function of V_{GT}, where V_{GT} is given by $V_{GS} - V_{TH}$.

Observing figure 4, for the same V_{GT}, drain current with the internal drain configuration is higher than the external drain configuration, because of the pinch-off point behavior in the CGT as explained before. Besides, the CGT with the external drain configuration presents similar behavior of the rectangular gate transistor. For $V_{GT} > 0.75$ V, the CGT drain current with both configurations is smaller than the conventional one, due to the mobility degradation in the CGT, because the drain current occurs in all directions in contrast to the conventional transistor (the mobility depends on the crystallography orientation). These characteristics are observed for different V_{DS} values ($0.1 \text{ V} \leq V_{DS} \leq 1$ V).

3. HARMONIC DISTORTION ANALYSIS

The linearity study is performed in the saturation region ($V_{GT} \leq V_{DS}$) and figure 5 presents the CGT and the conventional SOI nMOSFETs THD-V_{GT} curves for different values of V_a. They are extracted applying the IFM method.

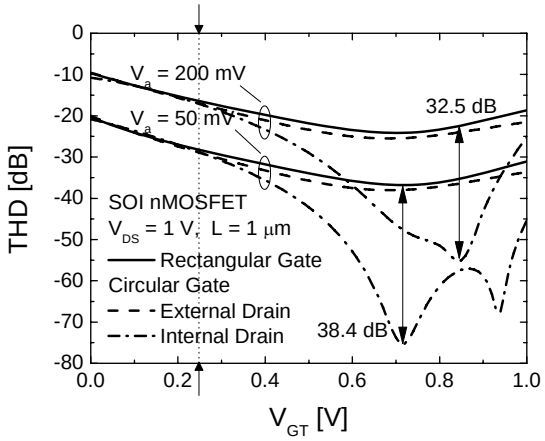

Figure 5 – THD versus V_{GT} of rectangular and circular gate SOI nMOSFETs for V_a equal to 50 mV and 200 mV.

The THD behavior is similar for all devices when $V_{GT} < 0.25$ V. When V_{GT} is higher than 0.25 V, the CGTs (mainly the internal drain) present lower THD than the rectangular gate. For $V_a = 200$ mV and $V_{GT} = 0.85$ V, the THD of the CGT with the internal drain configuration is lower than the external drain configuration and the rectangular gate for about 32.5 dB and 31.9 dB, respectively. The same THD behavior is observed considering $V_a = 50$ mV and $V_{GT} = 0.72$ V. Additionally, for $V_{GT} > 0.9$ V, it can be seen that the THD of the CGT with the internal drain configuration increases strongly due to the mobility degradation.

Figure 6 shows the CGT and the conventional HD3 behaviors for $V_a = 200$ mV.

Analysing it, we conclude that the $HD3_{CGT}$ is dominant when V_{GT} is smaller than 0.25 V (A region) and V_{GT} is higher than 0.68 V (C region), respectively. While the $HD3_{Rectangular\ Gate}$ is dominant into the interval given by $0.25 \text{ V} < V_{GT} < 0.68$ V (B region). The same HD3 behavior is observed for all transistors, with different V_a values.

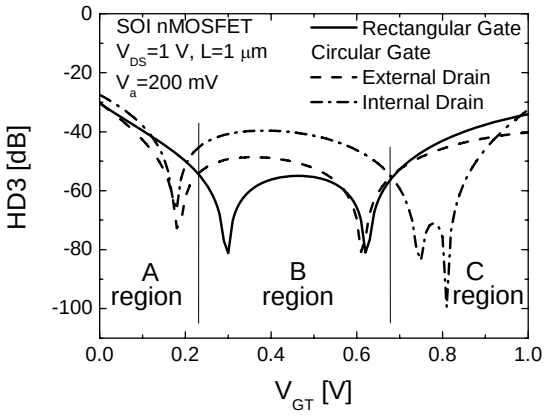

Figure 6 – HD3 versus V_{GT} of rectangular and circular gate SOI nMOSFETs for $V_a = 200$ mV.

4. CONCLUSIONS

It is observed that the circular gate transistor presents lower Harmonic Distortion or higher linearity than the conventional SOI nMOSFET in the saturation region. Besides, the CGT linearity behavior with external drain configuration is a little better than the conventional one. The CGT linearity behavior with the internal drain configuration is extremely superior than the conventional SOI nMOSFET for $V_{GT} > 0.5$ V. Knowing that high frequency amplifiers operate in strong inversion, the CGT with internal drain configuration can be used instead of the conventional one to improve extremely the Harmonic Distortion in analog applications.

The $HD3_{CGT}$ is dominant when V_{GT} is lower than 0.25 V (in direction of the weak inversion region) and when V_{GT} is higher than 0.68 V (in direction of the strong inversion region), when $V_a = 200$ mV.

5. ACKNOWLEDGEMENTS

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