# RADIATION INFLUENCE ON SOI CMOS DEVICES

*M. D. V. Martino, M. Sandri, P. G. D. Agopian, M. Galeti, W. A. M. Van Noije, J. A. Martino*

Laboratório de Sistemas Integráveis – LSI / PSI / USP – University of São Paulo
Av. Prof. Luciano Gualberto, trav. 3, n° 158, 05508-900 – SP – Brazil
mdvmartino@uol.com.br; m.sandri@uol.com.br

## ABSTRACT

This work presents the impact of different doses of radiation on SOI CMOS devices, exemplified by a classic inverter circuit. After the individual electrical characterization and the suitable extraction of parameters related mainly to the threshold voltage, carriers mobility, impact ionization and body effect for both the PD SOI nMOSFET and the FD SOI pMOSFET transistors, each transistor and the inverter circuit were simulated confirming the model fidelity to the experimental results. Based on these studied parameters, the inverter static transference curve was carefully analysed, also considering the relevant Kink Effect influence in function of different doses of radiation. From the simulations, it was obtained that the inverter transition voltage decreases approximately 0.3 V for a radiation dose of 100 krad. Meanwhile, the high noises margin increases also 0.3 V and the low noise margin decreases 0.2 V.

## 1. INTRODUCTION

The SOI ("Silicon-On-Insulator") MOSFET has been increasingly used during the last decade, mainly because of the very important advantages caused by its structure due to the presence of the buried oxide layer under the thin silicon film [1]. Besides the great potential to be used in integrated circuits in ultra large scale of integration (ULSI), these components are much more convenient in harsh environments, in which low sensitivity to temperature variation [2,3] and high hardness against transient radiation effects are required [4,5].

This mentioned remarkable hardness is essentially caused by the effect of the buried oxide layer, which isolates the active region of this kind of transistor, dramatically reducing or even eliminating undesirable effects caused by events such as single-event upset, single-event latchup and many others.

One of the major niche markets of these devices is the aerospace field, once that it is absolutely essential the use high hardness components, even when exposed to ionizing radiation. After all, because of the lack of the atmospheric protection, radiation can induce strong ionization, even inside the spacecrafts [6].

The goal of this work is to study the radiation influence on SOI CMOS inverter circuits up to 100 krad.

## 2. DEVICES AND SIMULATIONS

This work makes use of SOI MOSFET transistor fabricated in an 1 μm SOI CMOS technology in the Interuniversity MicroElectronics Centre (IMEC), Belgium. This technology uses 20, 400 and 180 nm of gate oxide, buried oxide and silicon film thickness, respectively. The PD SOI nMOSFET transistor is enhancement-mode, while the FD SOI pMOSFET one is accumulation-mode and both of them have a 20 μm channel width (W).

In order to simulate the radiation effects in transistors and inverter circuits, the AIM SPICE with the BSIM3 SOI model was used. The parameters inserted in the performed simulations were experimentally obtained through the nMOS and pMOS SOI transistors with different dimensions [7].

## 3. ELECTRICAL CHARACTERIZATION

The parameters extraction of the studied transistors was based on the curves of the drain current as a function of the gate voltage ($I_D$ x $V_{GS}$) and the drain current as a function of the drain voltage ($I_D$ x $V_{DS}$) for both the nMOS and the pMOS SOI transistors. The experimental data were obtained by making use of the semiconductor parameters analyzer Agilent 4156C.

Therefore, it was possible to extract many relevant intrinsic parameters, such as the threshold voltage ($V_{th}$), obtained through the second derivative method and the maximum carrier mobility ($\mu_o$), obtained in function of the maximum of transconductance curve in the linear region. In addition, the effective channel length ($L_{eff}$), determined with the transconductance for different gate mask length, and the mobility degradation coefficient ($\theta$) were also extracted. Particularly for the pMOS transistor, it was possible even to evaluate the short channel effect from the threshold voltage variation for different mask length values. Finally, the substrate doping concentration was estimated based on the electrical characteristics of the transistor and some previously extracted features, namely the threshold voltage.

Once all these parameters had been obtained, the simulation of these devices was performed considering its particular characteristics, such as maximum mobility, effective mobility degradation rate ($\theta$) depending on the perpendicular electric field and its physical features.

Based on the comparison between the simulated and the experimental data, some significant parameters were

fitted, so that the simulation became stricter to the transistor real behavior.

The adjustment based on the comparison between the simulated and the experimental nMOS $I_D$ x $V_D$ curve is necessary to take into consideration the Kink Effect through impact ionization and body effect parameters.

The Kink Effect occurs in partially depleted SOI nMOSFET transistors since, as the drain voltage raises in the saturation region, the body potential tends to increase, due to a migration of holes caused by impact ionization. Therefore, the threshold voltage decreases, resulting in an increase of the drain current, abruptly changing the $I_D$ x $V_D$ standard format [8], as can be observed in Figure 1.

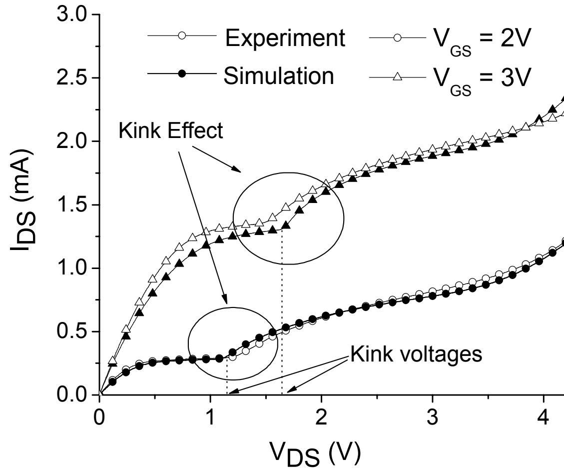


Figure 1 – Drain current ($I_{DS}$) as a function of the drain voltage ($V_{DS}$) for nMOS transistor with L=1μm and W=20μm.

## 4. LOGIC INVERTER CIRCUIT

After the transistors characterization, these devices were used in order to analyze the classic inverter circuit.

First of all, the experimental data, once more obtained using the mentioned semiconductor parameters analyzer, were compared to the simulated ones, with the previously extracted and adjusted parameters, confirming the reliability of the defined model, as it is shown in Figure 2.

Consequently, it was possible to extract the inverter transition voltage ($V_{Tinv}$) and the noise margins, following this procedure for three different inverter configurations, varying the channel length dimensions.

Analysing all the mentioned curves, it is clear, at first, the dependence of $V_{Tinv}$ from the $L_N/L_P$ ratio. This may be explained because when $L_N/L_P$ increases the gain factor $\beta_N/\beta_P$ declines, causing the expected $V_{Tinv}$ increase, as it is suggested by the classical transition voltage equation (eq. 1). As a result, the low noise margin ($NM_L$) is reduced and the high noise margin ($NM_H$) raises, as it is shown in Figure 2.

$$V_{Tinv} = \frac{V_{DD} + V_{th_P} + V_{th_N} \cdot \sqrt{\frac{\beta_N}{\beta_P}}}{1 + \sqrt{\frac{\beta_N}{\beta_P}}} \qquad (1)$$

where $V_{th_P}$ and $V_{th_N}$ are the pMOS and nMOS threshold voltage, and $\beta_P$ and $\beta_N$ are the pMOS the nMOS gain factor, respectively.

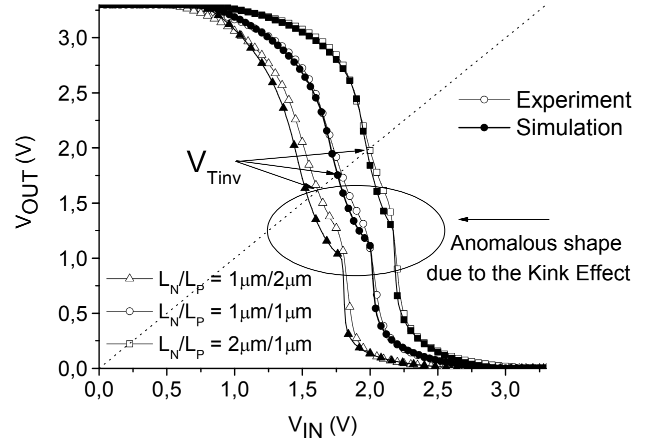


Figure 2 – Inverter output voltage ($V_{OUT}$) as a function of input voltage ($V_{IN}$) for three different $L_N/L_P$ ratios.

Besides that, the Kink Effect influence may be noticed in all of the curves, since the impact ionization that causes a significant change in the nMOS current level in the $I_D$ x $V_D$ graph generates the remarkable alteration in the static transference curve. It is evident that the abrupt change in the mentioned curve happens when the output voltage, which corresponds to the nMOS transistor drain voltage, is equivalent to the Kink voltage.

Finally, it is noticeable that the Kink Effect is responsible for a reduction in the inverter transition voltage. This result is clear in Table 1, in which the experimental data may be compared to the theoretical values, obtained from the classical transition voltage equation (eq. 1), which does not take the studied effect into consideration.

Table 1 – Theoretical and experimental inverter transition voltage ($V_{Tinv}$) for different $L_N/L_P$ ratios.

| | $V_{Tinv}$ (V) | |
|---|---|---|
| $L_N$ / $L_P$ | Equation 1 (without Kink Effect) | Experimental (with Kink Effect) |
| 1μm / 2μm | 1.76 | 1.54 |
| 1μm / 1μm | 1.92 | 1.76 |
| 2μm / 1μm | 2.05 | 1.98 |

## 5. RADIATION INFLUENCE

At last, the circuit was simulated under different doses of radiation. The radiation effect was modeled considering the variation in the threshold voltage as the most significant impact, as it is shown in Table 2.

The threshold voltage variation for these devices was based on reference [9]. According to the mentioned data resource, devices were irradiated with a $^{60}$Co, with exposures doses of 0, 10, 50 and 100 krad, after a 5 krad/hour dose-rate.

Table 2 – Threshold voltage after radiation [9]

| Dose (krad) | $V_{th}$ (nMOS) (V) | $V_{th}$ (pMOS) (V) | |
|---|---|---|---|
| | L=1μm or L=2μm | L=1μm | L=2μm |
| 0 | 1.27 | -0.44 | -0.54 |
| 10 | 1.26 | -0.64 | -0.74 |
| 50 | 1.17 | -0.89 | -0.99 |
| 100 | 1.07 | -0.99 | -1.09 |

Using the parameters previously determined, three simulations were performed with the AIM SPICE for each of the $L_N/L_P$ ratios, considering the mentioned doses of radiation and their consequents alterations in the threshold voltage. The simulated results for $L_N=L_P=1\mu m$ are shown in Figure 3.

Analyzing the plotted curves, it was clear that the inverter transition voltage declines as the radiation dose raises. This phenomenon occurs because the buried oxide charges increases due to the radiation impact. Accordingly, the low noise margin decreases and the high noise margin increases. It is relevant to notice that the $NM_H$ variation is clearly more significant than the $NM_L$ one. This occurrence is justifiable because $V_{th_P}$ is, indeed, much more susceptible to the radiation influence than $V_{th_N}$.

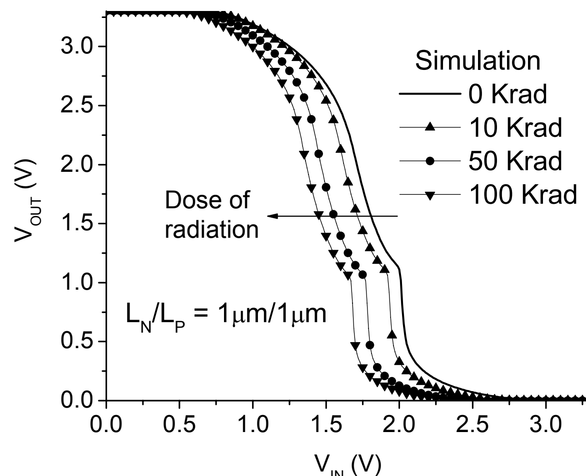


Figure 3 – Output voltage ($V_{OUT}$) as a function of the input voltage ($V_{IN}$) for different radiation doses.

Besides that, it is possible to compare the simulated inverter transition voltage variation with the theoretical ones obtained with equation (1), as it is shown in Figure 4. It is clear, then, that the theoretical calculations, even without considering the Kink Effect, show the same tendence as the radiation dose increases. In addition, the inverter transition voltage variation is clearly more relevant for the $L_N / L_P$ = 2 μm /1 μm configuration, when the $\beta_N / \beta_P$ ratio is lower. This consequence is expectable since mathematical analysis of equation (1) reveals that if $\beta_N/\beta_P$ decreases, $V_{Tinv}$ increases for the same value of $V_{th_P}$ and $V_{th_N}$.

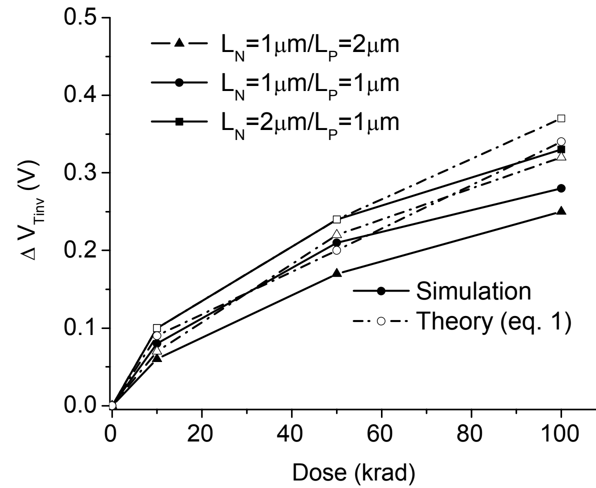


Figure 4 – Transition voltage variation as a function of the radiation doses for different $L_N/L_P$ ratios.

Finally, it is interesting to notice that, considering the simulated radiation doses, the percentage variation of threshold voltage was virtually the same for all the studied $L_N / L_P$ dimensions, as it is shown in Figure 5.

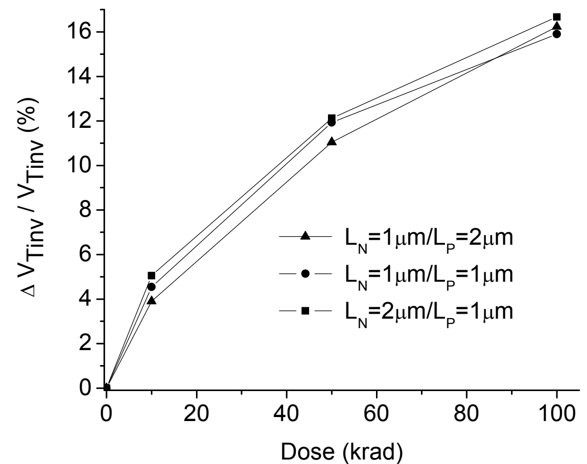


Figure 5 – Percentage variation of threshold voltage as a function of radiation doses for different $L_N/L_P$ ratios.

## 6. CONCLUSION

In this work, the radiation influence on SOI CMOS devices was studied after a careful analysis of the Kink Effect impact on inverter circuits.

Firstly, it was concluded that the abrupt increase in the patially depleted nMOS transistor drain current causes a remarkable change in the static transference curve resulting in a relevant decline in the inverter transition voltage.

By simulating the previously defined transistors model, the radiation impact was analyzed for different $L_N$ / $L_P$ ratios and radiation doses. The results showed that the transition voltage tends to decrease approximately 0.3 V for a radiation dose of 100 krad, since the threshold voltage declines for both nMOS and pMOS transistors under radiation exposure.

As a final point, it was detected that the percentage variation of threshold voltage was considerably similar for all the analyzed configurations (approximately 16% for 100 krad), but, undoubtedly, the absolute variation is clearly more significant as the $L_N$ / $L_P$ ratio increases.

## 7. ACKNOWLEDGEMENTS

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