SHORT-CHANNEL EFFECTS IMPROVEMENT BY USING DOUBLE-GATE SOI MOSFET

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ABSTRACT

In this paper a comparison between short-channel effects in single and double-gate devices is presented. The analysis is carried out through two-dimensional numerical simulations, by comparing the threshold voltage, subthreshold slope and the DIBL effect in both structures, varying the channel length down to 0.25μm. The results show that double-gate devices present better short-channel effects behavior than single-gate devices. Technological parameters were varied, showing that short-channel effects are reduced with silicon film thickness reduction.

1. INTRODUCTION

In recent years, great attention has been dedicated to fully depleted (FD) SOI MOSFETs, mainly due to their significant advantages over conventional bulk MOSFETs for low-power low-voltage applications due to their steeper subthreshold slope, reduced body factor and larger drain current [1]. Besides, SOI devices are less susceptible to short-channel effects than conventional ones, due to the presence of the buried oxide that lies beneath the source and drain regions and are responsible for the reduction of the source-channel and drain-channel depletion regions [1]. However, as devices are scaled down, short-channel effects (SCE's) start happening, causing the rise of interest on double-gate (DG) transistors since they can provide better scaling properties in comparison to conventional single-gate (SG) devices. In this device, the presence of two inverted channels makes possible the use of smaller dimensions without the occurrence of short-channel effects, due to the better control of the channel charges [2]. Besides, when compared to single-gate devices, double-gate transistors provide quasi-ideal subthreshold slope, larger transconductance and drain current level at the same gate voltage (V_{GF}) [2].

In this work, short-channel effects occurrence in single-gate and double-gate FD SOI nMOSFETs are compared. The threshold voltage, subthreshold slope and DIBL effect (drain induced barrier lowering) were used to evaluate the improvement on short-channel effects occurrence provided by the double-gate transistor. The maximum transconductance extracted at low electric field is also shown. This study was performed through two-dimensional numerical simulations of SG and DG devices, varying technological parameters.

2. SIMULATION DETAILS

The two-dimensional numerical simulations were performed using Atlas program [3]. Physical models accounting for mobility dependence on electric field, velocity saturation and doping concentration, bandgap narrowing, Auger recombination and doping-dependent lifetime were included in the simulation files.

Figure 1(a) presents the cross-section of the simulated single-gate device, indicating thicknesses and bias terminals. The same structure was simulated including a second gate (Figure 1(b)) in order to compare its results to the single-gate counterpart.

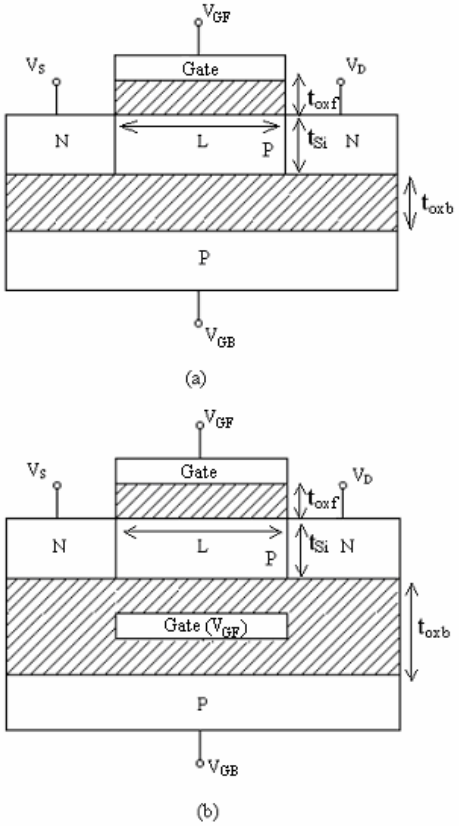

Fig. 1. Cross section of a (a) single-gate and (b) double-gate nMOS devices used in this work.

Single and double-gate devices were simulated with three different sets of technological parameters. The buried oxide thickness (t_{oxb}) and source/drain doping concentration (N_d) were 390nm and $1x10^{21}$ cm^{-3}, respectively, for all simulated devices. The other parameters (gate oxide thickness, t_{oxf}; silicon film thickness, t_{Si}; and channel doping concentration, N_a) are presented in Table I.

Table I. Simulated set of parameters

Parameters	***A***	***B***	***C***
Gate oxide thickness (t_{oxf}) [nm]	*40*	*30*	*15*
Silicon film thickness (t_{Si}) [nm]	*120*	*80*	*50*
Channel doping concentration (N_a) [cm^{-3}]	*$3x10^{16}$*	*$6x10^{16}$*	*$1.2x10^{17}$*

3. STUDIED SHORT-CHANNEL EFFECTS

Aiming to analyze the short-channel effects in SG and DG transistors, the channel length was varied from 10μm to 0.25μm for both device structures. In order to verify the influence of the double-gate architecture, this section presents the obtained results only for the second set of parameters (set B).

As already mentioned, the use of double-gate transistor improves the transconductance in comparison to the single-gate device. Figure 2 presents the maximum transconductance (GM,max) obtained through the peak of the drain current (I_{DS}) curve as a function of V_{GF} at drain bias (V_{DS}) of 50mV. From this figure, one can note that the presence of two gates promotes an increase of GM,max, which indicates that DG devices are able to promote a larger drain current variation for a given gate voltage variation independent of the channel length.

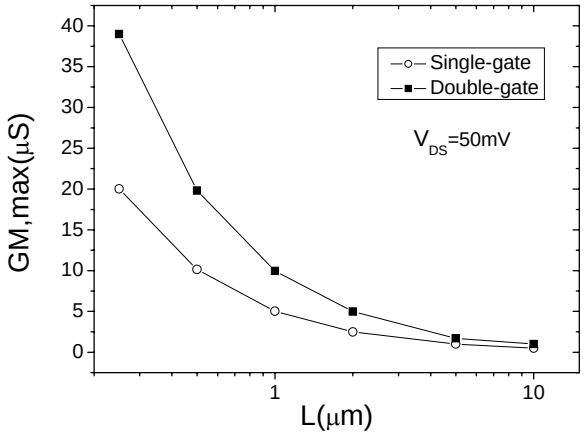

Fig. 2. Maximum transconductance in linear region as a function of channel length for single and double-gate devices.

3.1. Threshold voltage

The threshold voltage (V_T) was determined from the maximum point of the second derivative of the I_{DS} *versus* V_{GS} curves with small applied drain voltage (V_{DS}=50mV) [4].

Figure 3 presents the extracted V_T normalized by the threshold voltage of long-channel devices (V_{T0}) as a function of channel length for single and double-gate transistors. In this figure the percentage of V_T variation in comparison to V_{T0} ($\Delta V_T/V_{T0}$) is also presented for both structures. Figure 3 allows one to directly compare the threshold voltage reduction with L roll-off, which has shown to be smaller in double-gate devices. The percentage of V_T variation as a function of the channel length presented in logarithmic scale, stresses that this effect does not occur for long-channel devices and it becomes larger as the channel length is reduced. As expected, larger variations are observed for shorter devices. For the 0.25μm-long devices, the $\Delta V_T/V_{T0}$ is of 54.8% for the single-gate device while it is reduced to 25% for the double-gate one.

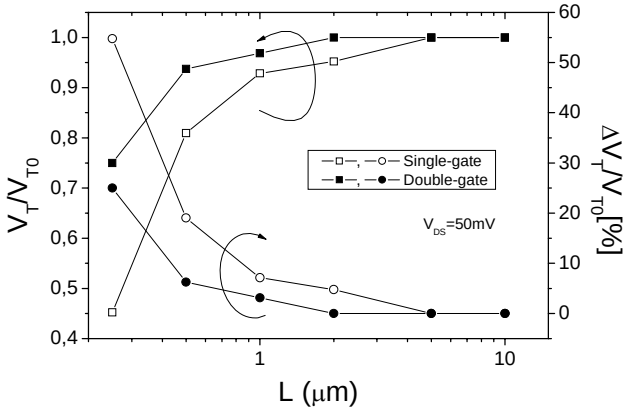

Fig. 3. Extracted V_T normalized by the threshold voltage of long-channel devices (V_{T0}) and percentage of threshold voltage variation ($\Delta V_T/V_{T0}$) of SG and DG devices as a function of channel length.

3.2. Subthreshold slope

The subthreshold slope (S) was extracted from the inverse of the subthreshold slope of I_{DS} *versus* V_{GS} curves in the subthreshold regime, presented on a semi-logarithmic plot. This parameter relates the gate voltage variation needed to increase the drain current in one decade. Ideally, the value of S for SOI devices is about 60mV/dec at room temperature [5].

Figure 4(a) presents the extracted subthreshold slope of SG and DG devices as a function of channel length. As can be noted from this figure, the subthreshold slope is virtually constant down to L=0.5μm. Also, the devices with two gates present lower percentage variation than the single-gate ones, as can be seen in Figure 4(b) that presents the percentage of S variation in comparison to the subthreshold slope of long-channel devices (S_0), $\Delta S/S_0$. For smaller devices, this variation reaches 60% for SG devices and 30% for DG ones. In practical terms, the lower the value of S, the more efficient and rapid the switching of the device from the off state to the on state.

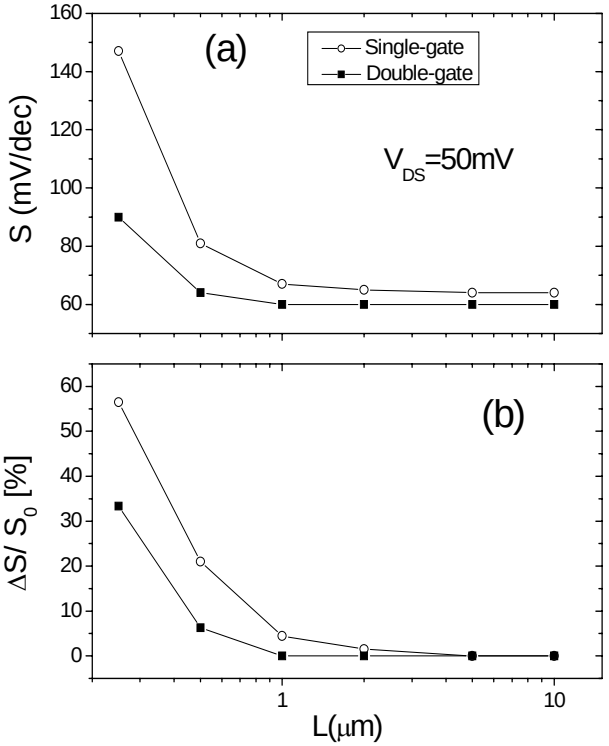

Fig. 4. Extracted subthreshold slope (a) and percentage of subthreshold slope variation (S/S_0) (b) of SG and DG devices as a function of channel length.

3.3. Drain-Induced Barrier Lowering (DIBL)

One of the most common ways to verify the occurrence of SCE's is to monitor the threshold voltage (V_T) variation with drain bias rise, which is called the drain-induced barrier lowering effect (DIBL)[2]. This effect happens because when the PN junction between drain-channel is reversed biased, the depletion region increases, reducing the total charge controlled by the gate, consequently reducing the threshold voltage [6]. For long-channel devices, this effect is suppressed, since the depletion region from source-channel and drain-channel regions are negligible in comparison to the charge controlled by the gate. On the other hand, this effect is more significant for shorter devices and can reach several mV. In this work, the DIBL was obtained through the difference of the threshold voltage extracted considering a constant current level of $I_{DS}=10^{-7}$ * (W/L) [A] with V_{DS}=50mV and V_{DS}=1.5V.

Figure 5 presents the extracted threshold voltage variation with drain bias as a function of the channel length. As expected, the DIBL effect is negligible for long-channel devices, both with single and double-gate architectures. As the channel length is reduced, it starts to be significant (near to 1μm). For the smallest simulated device (L=0.25μm), it was obtained a variation of about 600mV for the SG device and 250mV for the DG one, which means a reduction of nearly 58% in the difference [$V_T(V_{DS}$=50mV) - $V_T(V_{DS}$=1.5V)].

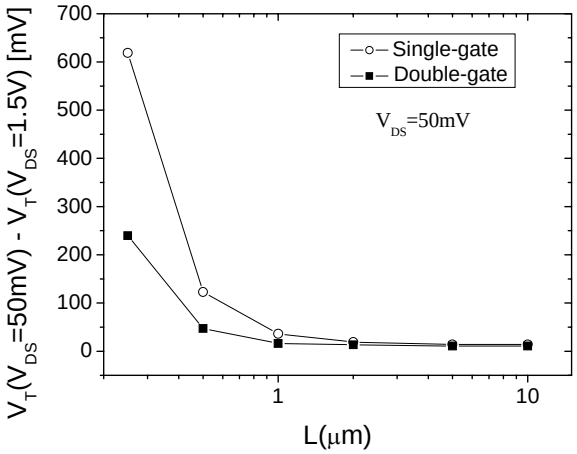

Fig. 5. Threshold voltage variation with drain bias as a function of channel length

4. TECHNOLOGY INFLUENCE ON THE SCE'S

In order to analyze the influence of different technological parameters on SCE's occurrence in double-gate and single-gate devices, numerical simulations were performed with the parameters shown in Table I.

Table II presents the percentage of variation of the threshold voltage for single and double-gate devices with two different channel lengths, for all sets of parameters. For the 2μm-long single-gate device, a small V_T variation was observed while in the double-gate one no variation in V_T was seen, showing the suppression of the short-channel effect. For shorter devices, the variation increases for both structures, but it is larger for the single-gate one. In all cases, the silicon film thickness reduction contributes to reduce the threshold voltage reduction, due to the larger amount of charge controlled by the gate.

Table II - Percentage of threshold voltage variation ($\Delta V_T/V_{T0}$) of SG and DG devices with L=2μm and L=0.25μm for the three simulated technologies.

	$\Delta V_T/V_{T0}$ [%]			
	L=2μm		**L=0.25μm**	
	SG	**DG**	**SG**	**DG**
Set A t_{Si}=120nm	5,6	0	88,9	63
Set B t_{Si}=80nm	4,8	0	54,8	25
Set C t_{Si}=50nm	0	0	33,3	12

In the analysis of the subthreshold slope behavior as a function of the technological parameters, it was also considered a long and a short-channel device. Table III presents the extracted values of S for each simulated technology and L=0.25μm and 5μm. As can be seen from the results, smaller variations are presented for long-channel devices and in the case of the double-gate one it reached the theoretical value (60mV/dec) for all silicon

film thicknesses. For the long-channel single-gate device it was observed a slight increase of S, which decreases with the silicon film thickness. For the device with L=0.25μm, one can see that both single and double-gate devices suffer from SCE's, marked by the increase of S. However, as expected, in the DG device, this S degradation is smaller than in the SG device. Also, as in the V_T analysis, a better control of the channel charge by the gate was attained for thinner silicon films [2].

Table III - Subthreshold slope extracted for single and double-gate devices with long (L=5μm) and short (L=0.25μm) channel length.

	Subthreshold Slope [mV/dec]			
	L=5μm		**L=0.25μm**	
	SG	**DG**	**SG**	**DG**
Set A t_{Si}=120nm	66	60	273	133
Set B t_{Si}=80nm	64	60	147	90
Set C t_{Si}=50nm	62	60	92	66

Figure 6 presents the percentage of S variation in comparison to the subthreshold slope of long-channel devices, $\Delta S/S_0$, as a function of t_{Si} for SG and DG devices with L=0.25μm. As can be seen, not only the absolute value of S is smaller at thinner silicon films, but also the percentage of variation reduces with t_{Si} roll-off: the percentage of variation is about 190% for t_{Si}=120nm and reduces to about 25% for t_{Si}=50nm.

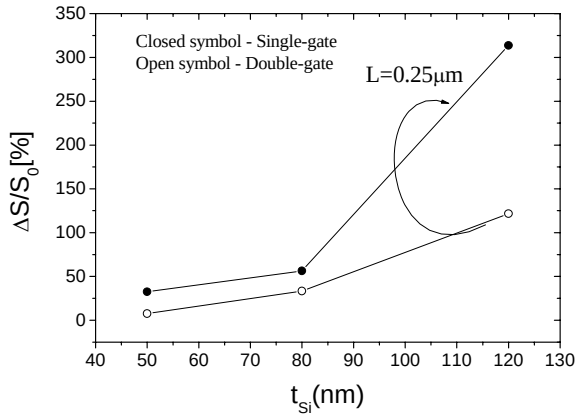

Fig. 6. Percentage of subthreshold slope variation (S/S_0) of SG and DG devices with L=0.25μm as a function of silicon film thickness.

The obtained results for the V_T variation caused by the DIBL effect in all simulated technologies with channel length varying from 0.25μm to 10μm are presented in Table IV. Once again one can note the lower threshold voltage variation with drain bias increase as the silicon film thickness is reduced, which is in agreement with data reported in ref. [2].

Table IV - Threshold voltage variation [$V_T(V_{DS}$=50mV) - $V_T(V_{DS}$=1.5V)] caused by the DIBL effect.

	$V_T(V_{DS}$=50mV) - $V_T(V_{DS}$=1.5V) [mV]					
	t_{Si}= 120nm (Set A)		**t_{Si}= 80nm (Set B)**		**t_{Si}= 50nm (Set C)**	
L (μm)	**SG**	**DG**	**SG**	**DG**	**SG**	**DG**
10	15	10	13,4	9,7	9	7,1
5	17	11	14	11	10	7,4
2	24	14	19	14	12,3	8,2
1	84	24	36	16	18,4	10
0.5	254	98	123	47	47	16
0.25	1220	510	619	240	205	53

5. CONCLUSION

This work presented an evaluation of short-channel effects improvement provided by the use of double-gate SOI nMOSFETs in comparison to single-gate ones. This analysis was performed by using numerical simulation results. Analyzing the obtained results, it is clearly seen that the double-gate structure presents improved SCE's behavior than the single-gate device. For long-channel devices this improvement is virtually negligible, but increases as the channel length is reduced. For short-channel devices, even double-gate transistors present SCE's but it is less pronounced than in single-gate transistors. The reduction of the silicon film thickness showed that there is an increase of the control of the device for both single and double-gate transistors, promoting the improvement on the devices behavior regarding SCE's. In the case of double-gate devices there is also an improvement due to the better coupling between the two gates.

6. REFERENCES

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