RING VOLTAGE CONTROLLED OSCILLATORS FOR AN RF TRANSCEIVER

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ABSTRACT

In this paper, two voltage controlled oscillators were designed and characterized in order to validate the proposed circuit architecture to be used in the radio transceiver of a reconfigurable SoC for animal and vegetable tracking. A full version of both circuits was fabricated using AMS CMOS 0.35μm technology.

1. INTRODUCTION

The increasing food export activity in global scale presents various challenges to producers. When it comes to perishable goods such as fresh fruits, the maintenance of adequate environmental transport conditions is a crucial goal. Tracking a fruit load throughout its whole export chain is an essential requirement to assure the product quality to its end consumer. The strategy proposed by our institution team consists of adopting wireless sensor networks distributed inside the fruit packages in a cargo container to monitor fruit samples and the container environmental conditions in order to evaluate the cargo conditions along its transport chain. A communication and local supervision module (also attached to the transport vehicle) integrates the data gathered by the sensor network and provides status reports via terrestrial monitoring stations placed along the transport route or via the satellite link also used for the transporter global positioning tracking. The embedded supervision unit may also generate alarm signals whenever the cargo might be under hazardous transport condition.

Each node of the network will be composed by a pseudo-fruit containing a reconfigurable SoC and some sensors (humidity, temperature and acceleration). The embedded rSoC should be able to communicate with other components of the network using a RF interface. This interface is specified to operate in the ISM 900MHz band using a very simple ASK modulation half-duplex scheme.

This paper presents the design and characterization of two VCOs based on a ring oscillator architecture. The paper outlines as follows: Section 2 describes the VCOs design, Section 3 presents the layout of the structures, Section 4 shows the modules characterization and results, and 5 presents the conclusions.

2. VCO DESIGN

A ring oscillator is made by connecting an odd number of digital inverters in series with positive feedback. The oscillating frequency is given by the number of inverters (n) and the average delay time (td) needed by each inverter to switch from one state to another [1].

$$f = \frac{1}{2 \cdot n \cdot t_d} \tag{1}$$

In order to control the oscillating frequency, it was chosen, in this topology, to add a capacitor and a variable resistor in parallel with every inverter. Considering that each inverter can supply a fixed current and that the inverter switches after its input voltage has exceeded a threshold voltage, changing the value of the resistor deviates a controllable part of that current into the capacitor. If it deviates a large part, the available current to charge the input capacitance of the next inverter stage is small. It will need, then, a longer period of time to achieve such threshold voltage, decreasing the output frequency. A linear relation was expected between control voltage and output frequency, since the variable resistors were implemented using transistors in the triode region, in such way that the current through the transistors varies linearly with Vgs for a fixed Vds [2].

As the transceiver has the greatest power consumption in an rSoC application, the possibility of turning down the oscillator is very important. In order to control power consumption, an ENABLE pin was added to the circuit, allowing the CPU to turn the VCO down even if the supply voltage is on.

If ENABLE = 1, the NAND gate works as if it were a simple inverter, resulting in an odd number of inverters in series with positive feedback. When ENABLE = 0, the output of the NAND gate is always 1 despite what may come through the other input. The result of this alternative output is an even number of inverters, which causes the

circuit not to oscillate, even though the polarization has not been removed.

Digital CMOS devices are built to consume power only when they switch between two states. Taking that into account, the CPU can reduce the consumption nearly to zero if desired.

The first voltage controlled oscillator (VCO) was designed using digital AMS logic gates and it was named vco_0813. As these gates are optimized in frequency response, power consumption and area, they seemed a very good option for the VCO final circuit. Actually, during the simulation process, this circuit consumed only 460uW in steady state. This VCO was made by four optimized AMS inverters and an AMS NAND gate to insert the ENABLE signal. The schematic of this circuit is shown in Figure 1.

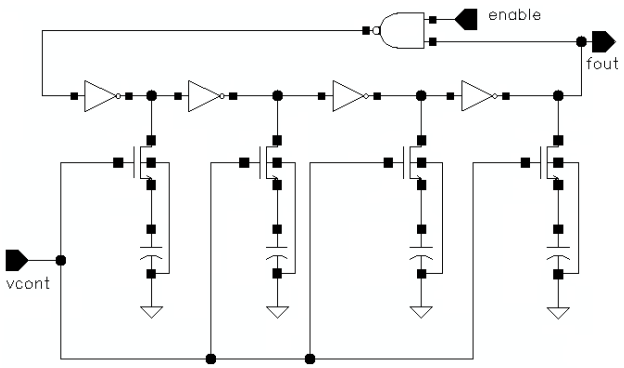

Figure 1: Schematic of vco_0813.

After the simulation process, it was possible to observe that the VCO gain, i.e. the frequency variation due to control voltage variation, was too large, making the PLL feedback implementation difficult [3]. Because of that, another VCO, named vco_0903, was designed using customized push-pull inverters and a customized NAND gate using the same circuit topology. Because of the customization, the circuit consumed 2.27mW during simulation, almost five times the power consumed by vco_0813. Although it consumes a lot more power, there are still some advantages like the desired smaller VCO gain. The schematic is shown in Figure 2.

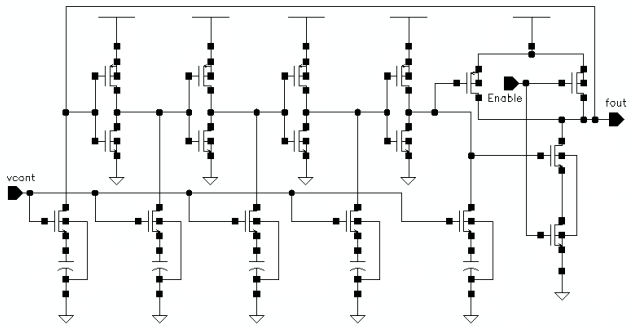

Figure 2: Schematic of vco_0903.

3. LAYOUTS

The layouts were drawn using CADENCE Virtuoso XL Layout Editor and checked using ASSURA DRC and LVS.

The layout of vco_0813 is shown in Figure 3.

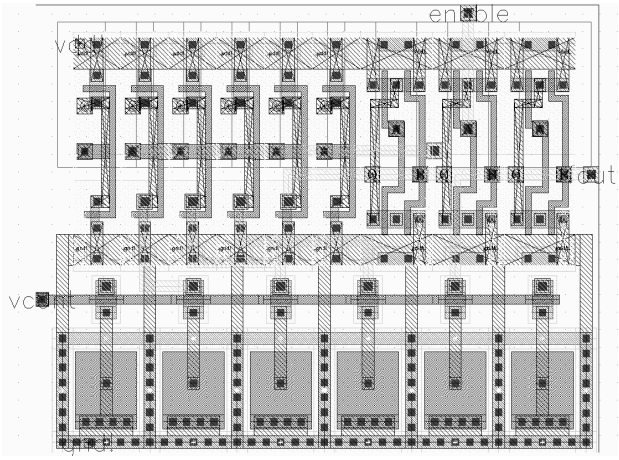

Figure 3: Layout of vco_0813.

As it can be seen, the AMS inverters and NAND gate are optimized making the whole layout very dense. Dummy structures such as inverters, capacitors and transistors were added to increase matching. The dimensions of this layout are 33um x 25.5um.

The layout of vco_0903 is shown in Figure 4. The dimensions of this layout are 35.6um x 24um. Dummy structures were also included to increase matching.

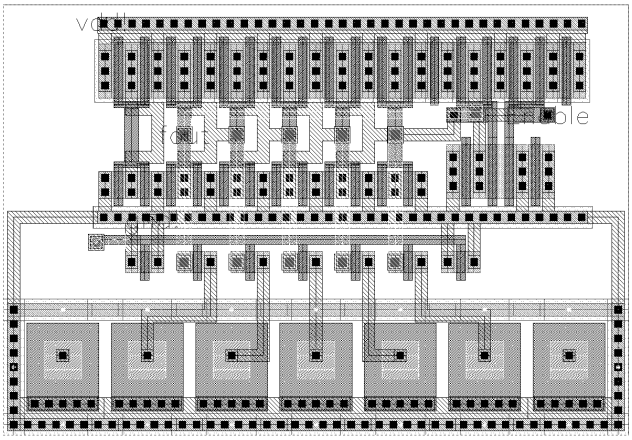

Figure 4: Layout of vco_0903.

4. CHARACTERIZATION

Both VCOs presented in this paper were prototyped in AMS 0.35um using CADENCE software and the characterization was made using a CASCADE probe station and a Rohde-Schwarz spectrum analyzer. The frequency x voltage characteristic for vco_0813 is shown in Figure 5.

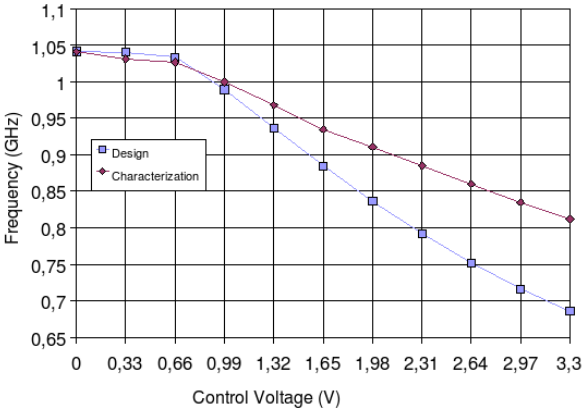

Figure 5: Simulated and measured characteristic of vco_0813.

As Figure 5 shows, there are two regions in the graph: in the first one, from 0 to approximately 0.7V, the output frequency is weakly dependent of the control voltage; in the second one, from 0.7V to 3.3V the frequency is linearly dependent of the control voltage. This was expected since a transistor with threshold voltage equal to 0.7V in triode region was used to implement the variable resistor. Figure 5 shows that the measured frequency of the ring oscillator was very close from the expected, but the gain showed a remarkable difference. Because of the small size of the components, the relative process variation was severe within the analyzed sample. This was expected from MONTE CARLO simulation.

Figure 6 presents the screen of the spectrum analyzer for the test of vco_0813. According to simulation, the signal 3dB bandwidth should be around 2.5MHz, but Figure 6 shows it is actually on 3.1MHz. Such result may be for two reasons: it may come from unforeseen effects of the output buffer that is very large, or, again, process variation may have affected the circuit severely. The measured phase noise for this circuit was -80dBc/Hz at 600kHz away from the maximum.

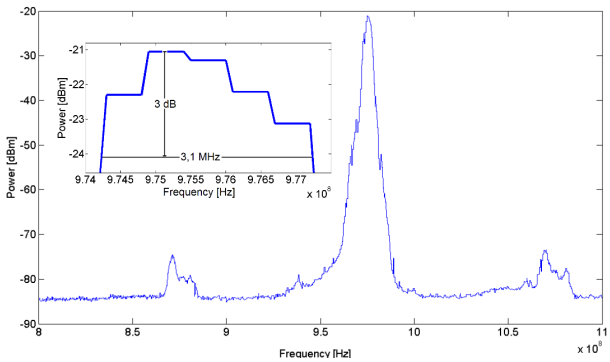

Figure 6: Spectrum of vco_0813 in wide band and in narrow band showing the peak.

The frequency x voltage characteristic for vco_0903 is presented in Figure 7, in which the same two regions from Figure 5 can be observed, although the oscillating frequencies are shifted because of process variation. The gain did not change significantly, but the offset frequency deviated more than 200MHz in the studied sample. This kind of deviation was also predicted using MONTE CARLO simulation.

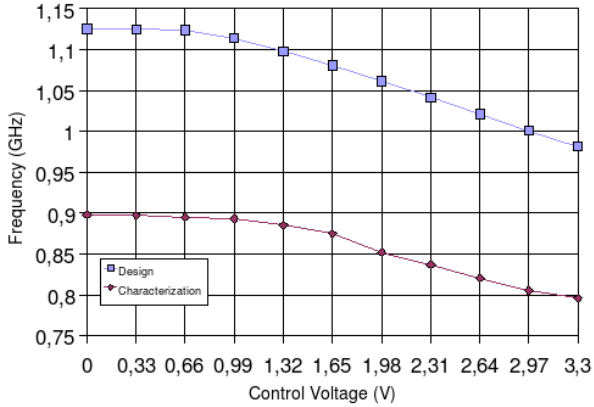

Figure 7: Simulated and measured characteristic of vco_0903.

Figure 8 presents the screen of the spectrum analyzer for the test of vco_0903. According to simulation, the signal 3dB bandwidth should be around 2MHz, but Figure 8 shows it is actually on 3.3MHz. The measured phase noise for this VCO was -82dBc/Hz at 600kHz away from the peak.

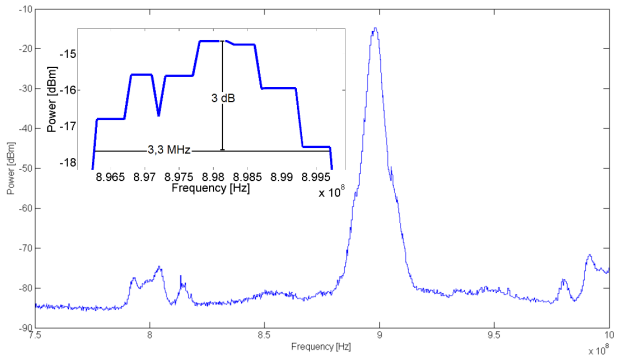

Figure 8: Spectrum of vco_0903 in wide band and in narrow band showing the peak.

5. CONCLUSION

Two ring VCOs were designed, prototyped and characterized. The first VCO made use of AMS digital gates, and presented very low power consumption but larger bandwidth and gain. The second one made use of customized digital gates, and presented better bandwidth, gain, but larger power consumption. Both VCOs were severely affected by process variation during fabrication.

6. REFERENCES

[1] LEE, T. H., The Design of CMOS Radio-frequency Integrated Circuits, Cambridge University Press, 1998.

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[3] SOARES, R. R. P., *Sintetizador de freqüência para transceptor de RF integrado em um SoC CMOS*, UnB, Brasilia DF, Brazil, August 2005.