STUDY OF HIGH TEMPERATURE INFLUENCE ON MOS CAPACITOR HIGH FREQUENCY C-V CURVES BEHAVIOR

Ana Paula Borges Ziliotto and Marcello Bellodi

Department of Electricity, Centro Universitário da FEI, São Bernardo do Campo,
São Paulo – 09850-901, Brazil

ABSTRACT

It is presented numerical bi-dimensional simulations results concerning the high frequency capacitance versus voltage (C-V) characteristic of the MOS capacitor operating from room temperature up to 573K using AC analysis. The results show that the C-V curves behavior is influenced by substrate doping concentration, substrate and gate materials. Also, it is presented experimental results concerning to the high frequency C-V characteristic of a sample MOS capacitor, confirming the results obtained through simulations.

INTRODUCTION

The increasing utilization of MOS devices in applications involving high temperature environments has demanded for further knowledge on components behavior up to 573K.

The study of C-V curves behavior in harsh environmental conditions is subject of great interest for electronic controls employed on avionics, internal combustion engines and geothermal oil wells applications, which are currently the most demanding markets for reliable high temperature silicon based devices [1, 2, 3, 4].

It is a fact that the overall cost of electronic devices applied to automobiles and airplanes can be expressively reduced if they can operate directly in hot areas [1, 2, 3, 4]. This would also eliminate the necessity of insulation and cooling mechanisms or devices to maintain the temperature within the limits tolerated by silicon, currently around 398K [1].

The MOS capacitor was selected to be studied n this context, especially due to its simple structure and presence in almost every MOS device, being he elementary MOS transistor structure.

The MOS capacitor structure is shown in figure 1, which is composed by a metal gate, an insulator layer and a semiconductor substrate which enables, through the simulated capacitance versus gate voltage curves, the study of various effects caused by the temperature increase.

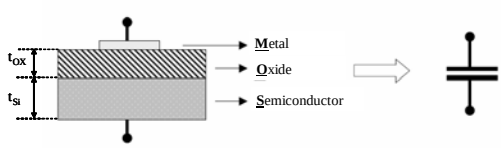

Figure 1. MOS capacitor structure and equivalent representation.

In this paper, the results presented were obtained through bi-dimensional simulator ATLAS [5]. The high frequency C-V curves were analyzed for a temperature range starting at room temperature (300K) and raised up to 573K.

For each group of curves, some parameters were analyzed in order to demonstrate the temperature influence on C-V characteristics such as the silicon substrate doping concentration, the substrate material type, the poly-silicon gate doping concentration and the gate material type.

BI-DIMENSIONAL NUMERICAL SIMULATION RESULTS AND ANALYSIS

The MOS capacitor used during the simulations performed for this study is composed by a N-type poly-silicon gate with doping concentration of $N_D=1x10^{21}$ cm^{-3}, a SiO_2 insulator layer with t_{ox}=2.5 nm, a P-type silicon substrate with doping concentration $N_A=5x10^{17}$ cm^{-3} and substrate layer of t_{Si}=600 nm thickness. The channel length (L) and width (W) were assumed to be 1 μm during all bi-dimensional simulations.

A DC voltage (V_G) was applied to the capacitor gate, varying from -3V to 3V and the AC analysis of high frequency C-V curve was performed, maintaining the frequency at 1 MHz for all simulations.

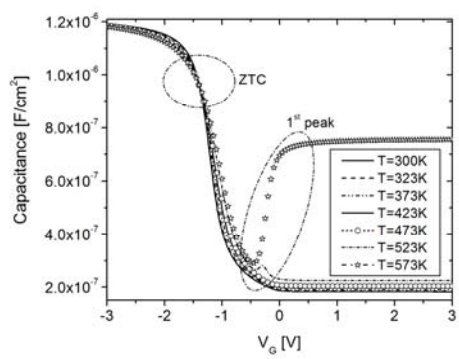

Figure 2. High frequency C-V curves for t_{ox}=2.5 nm, $N_A=5x10^{17}$ cm^{-3} and poly-silicon gate with doping concentration $N_D=1x10^{21}$ cm^{-3}, operating at high temperatures.

The first set of high frequency C-V curves is shown on figure 2. When a positive gate voltage is applied to the MOS capacitor structure ($V_G > 0$ V), the C-V characteristics for 473K temperature and up to 573K present a behavior tendency that diverges from the room temperature high frequency C-V characteristic. This is the inversion region and the tendency suggests that, although the frequency was maintained at 1 MHz, the curves approach a low frequency C-V curves behavior for higher temperature values.

The increase on the total capacitance value for $V_G > 0$ V indicates that there are physical effects influencing the MOS capacitor structure, more precisely in the silicon substrate, since the capacitance in the inversion region of the high frequency C-V curve is mainly due to the substrate depletion region, since the capacitance associated to the oxide layer does not change when t_{ox} is maintained constant.

Total capacitance is expressed by the series association of the oxide capacitance, which is constant for a given t_{ox} thickness, and the substrate capacitance that varies with the depletion region width (W_d). Figure 3 represents the series capacitances association.

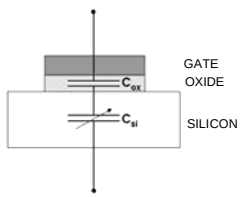

Figure 3. Series capacitance association of a MOS capacitor structure.

T is possible to note at the curves of figure 2 the ZTC point (Zero Temperature Coefficient),in which the device's electrical characteristics are identical, independent of the operating temperature.

The 1st peak indicated in figure 2 is due to the capacitance value increase in the silicon substrate during the device operation in the inversion region. In room temperature, this effect is not present as the carrier generation in the substrate does not suffer great influence of the temperature. Increasing the temperature, the thermal generation of carriers starts to take place in the silicon substrate and becomes the predominant mechanism of electron-hole pairs generation, causing intrinsic silicon carrier concentration (n_i) to increase exponentially with temperature [6, 7, 8]. The dependence of n_i with temperature is given by equation (1) [8, 9].

$$n_i = 3.9x10^{16} T^{3/2} e^{-Eg/2kT} \qquad (1)$$

When the device reaches the temperature of 573K, the intrinsic concentration assumes a value of n_i=3.9x10^{15} cm^{-3}, which is significantly greater than n_i at room temperature, which is approximately 1.5x10^{10} cm^{-3}.

These carriers that were thermally generated in the substrate assume an important role in the composition of the capacitance value in the inversion region of the MOS device, since the gate voltage V_G is no longer the only electrical effect controlling the minority carriers in the depletion region.

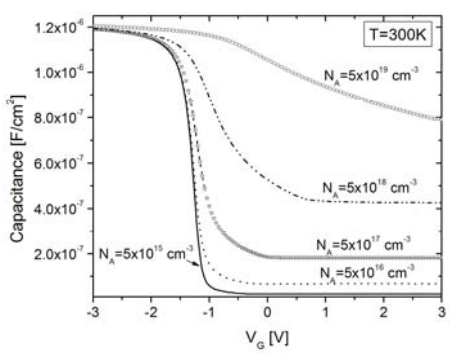

Figure 4. High frequency C-V curves for MOS capacitor with P-type substrate, poly-silicon N-type gate with concentration N_D=1x10^{21} cm^{-3} and oxide thickness t_{ox}=2.5 nm, for the substrate concentration varying from N_A=5x10^{15} cm^{-3} up to 5x10^{19} cm^{-3} at T=300K.

In order to investigate with more details the influence of the substrate implanted doping concentration (N_A) when the MOS capacitor is operating at elevated temperatures, the same device was simulated for different N_A values. Figure 4 shows some results for the MOS capacitor operating at 300K.

It can be observed by the tendency behavior of the C-V curves shown in figure 4 that the substrate concentration N_A influences the minimum capacitance value in the inversion region, which is expected since the silicon substrate capacitance in the depletion region depends on the maximum depletion region width (W_{dmax}), as shown by equation (2) [10] and (3) [7]. It is possible to conclude that the substrate doping concentration increase causes the inversion region total MOS capacitance to increase as well since the capacitance due to the silicon depletion region (C_{si}) is inversely proportional to the maximum depletion width (W_{dmax}).

$$C_{si} = \frac{\varepsilon_{si}}{W_{dmax}} \qquad (2)$$

$$W_{dmax} = \sqrt{\frac{2\varepsilon_{si} 2\phi_F}{qN_A}} \qquad (3)$$

Now in figure 5, it is possible to observe the C-V curves behavior as a function of the substrate concentration N_A varying from 5x10^{15} cm^{-3} up to 5x10^{19} cm^{-3}, operating at 573K.

Operation at elevated temperatures, as shown in figure 5, causes the presence of the 1st peak effect in the inversion region of the curves, due to the already mentioned increase of the silicon intrinsic carriers concentration. Low doping substrate concentration values, such as 5x10^{15} cm^{-3} and 5x10^{16} cm^{-3}, make the 1st peak effect approaches to the behavior of a typical low frequency C-V curve, where the total capacitance in the inversion region tends to be equal to the total capacitance observed in the accumulation region. This tendency can only be noticed due to the fact that, at 573K, the n_i value is practically the same as the N_A value for these low doping substrate concentrations, which causes the channel minority carriers to be influenced not only by the gate voltage applied to the MOS capacitor, but also by other substrate mechanisms that can not be controlled and are inherent to the silicon material.

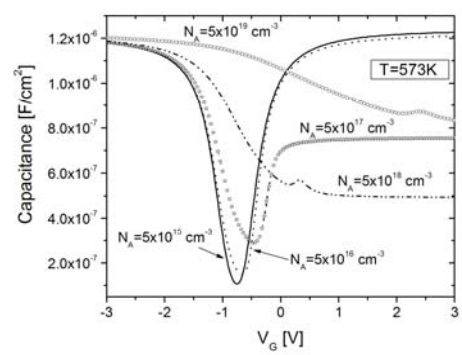

Figure 5. High frequency C-V curves for MOS capacitor with P-type substrate, poly-silicon N-type gate with concentration N_D=1x10^{21} cm^{-3} and oxide thickness t_{ox}=2.5 nm, for the substrate concentration varying from N_A=5x10^{15} cm^{-3} up to 5x10^{19} cm^{-3} at T=573K.

Aiming the investigation of the 1st peak effect in the inversion region on a real MOS capacitor sample, to validate all the simulated data up to this point, figure 6 presents the high

frequency C-V curves of a MOS capacitor measured since room temperature up to 573K.

Both the ZTC point and the 1st peak effect can be observed in the curves of figure 6, proving that the simulated curves obtained with ATLAS represent the MOS capacitor tendency behavior observed for elevated temperatures.

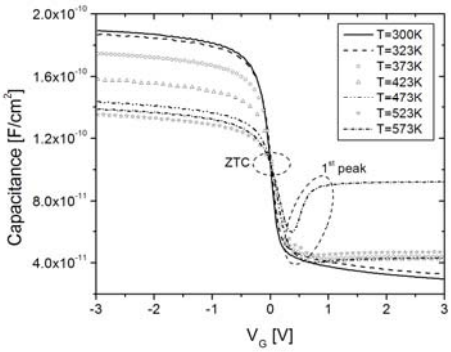

Figure 6. C-V curves for MOS capacitor with P-type substrate measured experimentally for high frequency of 1 MHz.

As the simulated results can represent a MOS device, the study continued with the investigation of other capacitor parameters and respective effects in high temperature.

The poly-silicon gate concentration variation was studied and the results are presented by figure 7, where it is shown three different poly-silicon concentration values at T=300K.

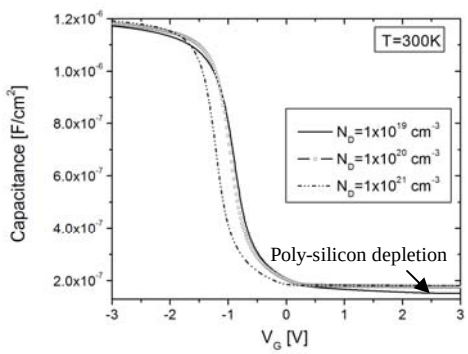

Figure 7. High frequency C-V curves for T=300K with poly-silicon gate concentration variation for t_{ox}=2.5 nm.

We can observe that the lower the poly-silicon concentration value N_D is, more evident is the effect of poly-silicon depletion in the inversion region of the high frequency C-V curve. This means that the total capacitance of the MOS device has the influence of a poly-silicon depletion region capacitance in series with the oxide and silicon substrate capacitances. Figure 8 shows the schematic representation of the MOS total capacitance in this case.

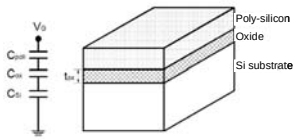

Figure 8. Equivalent model of the capacitance series association [10].

The depletion region that is formed in the poly-silicon gate influences the MOS capacitor behavior when the temperature reaches higher values, such as T=573K, as presented by figure 9.

It can be observed that, besides 1st peak effect, an additional 2nd peak is present on the C-V curves of figure 9, for V_G > 1.5V. The 2nd peak is not observed for poly-silicon higher doping concentration materials, which only demonstrates that the poly-silicon depletion region combined with the silicon substrate intrinsic carriers concentration increase cause the high frequency C-V curve degeneration in the inversion region. This effect shows that it is evident the correct choice for gate and substrate materials and concentrations are extremely important to avoid the negative influence of non controllable mechanisms inherent to the device materials when a MOS device is developed.

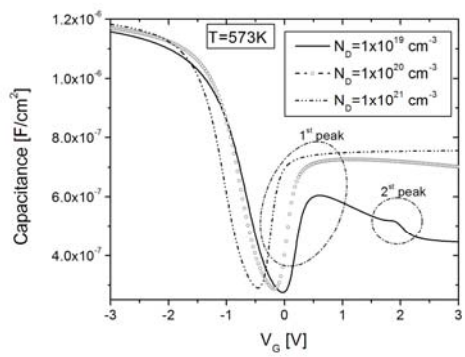

Figure 9. High frequency C-V curves for T=573K with poly-silicon gate concentration variation for t_{ox}=2.5 nm.

The ideal gate material for a MOS device, in order to avoid the gate depletion region influence, would be a metal. Figure 10 shows the high frequency C-V curves for T=573K for three different poly-silicon doping concentrations and also a metal gate, in this case the chosen material is the TiN.

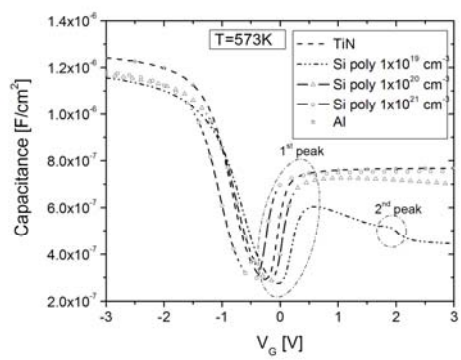

Figure 10. High frequency C-V curves for T=573K for some gate materials, for t_{ox}=2.5 nm.

The curve of the TiN material on figure 10 shows that when the gate is made of it, it does not contribute for C-V behavior degradation in the inversion region. The minimum capacitance value is constant for V_G > 0V, which can not be observed when the gate is composed by a low doped poly-silicon.

Another point investigated along this work was the substrate material influences on the C-V characteristic at high temperature. It is known that the band gap (E_g) is a semiconductor characteristic and silicon is considered a narrow

band gap material since its E_g=1.08 eV, when compared to diamond, whose E_g=5.45 eV [1, 5, 11, 12, 13].

Many researchers dedicate their studies to wide band gap materials as a replacement for silicon, aiming harsh environments applications [1, 11, 12, 13].

The MOS capacitor structure was then simulated for a silicon carbide (SiC) substrate, which is a wider band gap material than silicon and is currently being applied in the fabrication of MOS devices [1, 14, 15].

Figure 11 shows the high temperature behavior of the SiC substrate in a MOS device. It is observed that, at 573K, the band gap narrowing effect on the SiC is still not influencing the C-V curves in the inversion region, as observed for silicon substrate as presented in figure 2.

The intrinsic concentration value of the SiC substrate is not high enough at 573K to degenerate the minimum capacitance values for V_G > 0V, even when V_G is increased up to 10V, which is a condition we could never have in a real device, since it is an extremely high voltage for MOS devices which operate in analog/digital circuits.

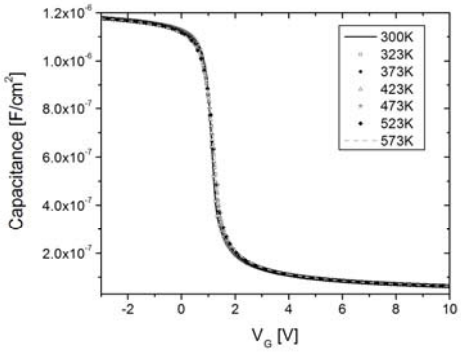

Figure 11. High frequency C-V curve for a MOS capacitor with SiC substrate at high temperatures.

The SiC and other wide band gap materials allow MOS devices to be designed for harsh environment applications, being more robust and precise structures when the temperature of operation is higher than 398K, which is most of MOS devices upper limit [1, 14, 15].

CONCLUSIONS

The high frequency C-V characteristic of a MOS capacitor, when operating at high temperatures, is influenced by the substrate material and doping concentration due to the band gap narrowing effect of the semiconductor and intrinsic carrier concentration increase as temperature begins to increase. There is also influence of the gate material and for poly-silicon, the doping concentration is also important to be taken into account because it degenerates the C-V curves in the inversion region due to the presence of a 2nd capacitance peak.

REFERENCES

[1] McDonnald, J.A., “Proving they can take the heat”, HTE Report, III-Vs Review, Vol. 9, No 5, pp. 63-67 (1996).

[2] Bellodi, M., Estudo das Componentes e Modelagem das Correntes de Fuga em Dispositivos SOI MOSFET Operando em Altas Temperaturas, Doctor Thesis, USP, São Paulo (2001).

[3] Grabinski, W., Stricker, A., Fichtner, W., “A Versatile Setup for Semiconductor Testing up to 550ºC”, HITEC 1998, USA, pp. 143-147 (1998).

[4] Osman, A.A., Osman, M.A., “Investigation of High Temperature Effects on MOSFET Transconductance (gm)”, HITEC 1998, USA, pp. 301-304 (1998).

[5] Device Simulation Framework, version 5.10.0.R, Silvaco International (2005).

[6] Sze, S.M., Physics of Semiconductor Devices, 2nd Edition, John Wiley & Sons, New York (1981).

[7] Streetman, B.G., Banerjee, S.K., Solid State Electronic Devices 6th Edition, Prentice Hall, New Jersey (2000).

[8] Colinge, J.P., Silicon-on-Insulator Technology: Materials to VLSI, 3rd Edition, Kluwer Academic Publishers, Massachusetts (2004).

[9] Muller, R.S., Kamins, T.I., Device Electronics for Integrated Circuits, 2nd Edition, Wiley, New York (1986).

[10] Rodrigues, M., Caracterização elétrica de capacitores obtidos através de tecnologia ultra-submicrométrica, Master Thesis, USP, São Paulo (2006).

[11] Chen, L.Y., McCluskey, P., “Microsystem Packaging for High Temperature Environments”, EEE Links, Vol. 8, pp.46-50, August (2002).

[12] McDonnald, J.A., “HiTec: International Focal Point for High Temperature Applications”, HTE Report, III-Vs Review, Vol. 9, Nº 4, pp. 57-59 (1996).

[13] Lande, S., “The E-MRS High Temperature Electronics Symposium”, Proceedings of Symposium E, Strasboug (1996).

[14] Prijic, Z., Pavlovic, Z., Ristic, S., Stojadinovic, N., “Zero Temperature Coefficient (ZTC) biasing of power VDMOS transistors”, Electronic Letters, Vol. 29, Nr. 5, March (1993).

[15] Eftimie, S., Rusu, A., “The influence of diffusion current on the Zero-TC point of a MOS transistor”, IEEE (2005).