DEVICE CHARACTERIZATION OF AN IBM 0.18µm ANALOG TEST CHIP

Giovano da Rosa Camaratta, Eduardo Conrad Jr, Luiz Fernando Ferreira,
Fernando Paixão Cortes, Sergio Bampi
{grcamaratta, econradjr, lfferreira, fpcortes, bampi}@inf.ufrgs.br

Federal University of Rio Grande do Sul (UFRGS) - Informatics Institute
Postal Code 15.064 – Zip 91.501-970 – Porto Alegre – Brazil

ABSTRACT

The design of an analog circuit depends on several factors such as good device modeling and technology characterization. In this context, in order to validate the design methodology and the electrical models of a target technology, electrical characterizations based on measurements are necessary. This paper presents the main modules and the initial characterization of a test chip developed with several RF blocks, oscillators and test devices. The chip was prototyped in IBM 0.18µm CMOS technology process through a MPW service. Preliminary measurements of the ring oscillator and test vehicles will also be presented.

1. INTRODUCTION

The development of ultra-scaled VLSI technologies, coupled with the demand for more signal processing integrated in a single chip, has set the trend for integrating analog circuits in digital CMOS technologies below 90 nm feature sizes.

Several analog circuit blocks were designed using a full-custom design methodology based on the g_m/I_D characteristics, the same methodology that was used in previous works [1]. In the first results, the technology characteristics and circuits performance were obtained with electrical simulations using the foundry-supplied typical BSIM3v3 model parameters for the target technology IBM 0.18µm CMOS technology.

In order to validate the design methodology and the electrical models, electrical characterizations based on measurements are necessary. Thus, a test chip was prototyped in IBM 0.18µm CMOS technology process and 10 not encapsulated chips and 5 encapsulated (64-pin QFN package) have been measured. The objective here is to use the electrical measurements to perform characterization to fine tune the basic design curves and validate the blocks performance.

2. TEST CHIP STRUCTURES

A test chip with the designed blocks and test vehicles in IBM 0.18µm CMOS technology was developed to characterize the design through electrical measurements. The chip microphotography is shown in figure 1 and the area of each block is shown in table 1. Each block that composes the test chip is briefly described as follows.

There are 6 RF analog building blocks implemented: a complete variable gain front-end architecture, an up-conversion mixer, a down-conversion mixer, a variable gain amplifier (VGA) [2] and a voltage-controlled oscillator (VCO) using a full-custom design methodology based on the gm/ID characteristics [3] and a ring oscillator. All the design optimizes both speed and the power consumption, as well as reasonable sensitivity and gain are achieved.

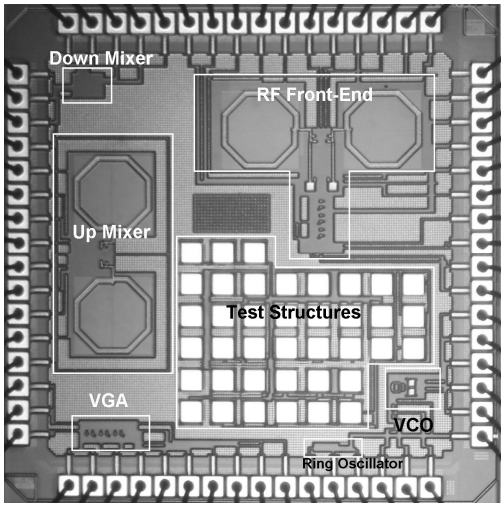


Figure 1 – Chip die microphotography.

Table 1 – System chip area breakdown.

Block	Area (mm^2)
Up Mixer FI=1.4GHz	0.7100
Down Mixer 1.4GHz to 40MHz	0.0210
VGA (Variable Gain Amplifier)	0.0350
RF Front-End	0.7700
VCO (Voltage Controlled Oscillator)	0.0220
Ring Oscillator	0.0073
Test Structures	1.2480
Pad Ring	1.7600
Unused Space	2.2260
Total Area	6.8000

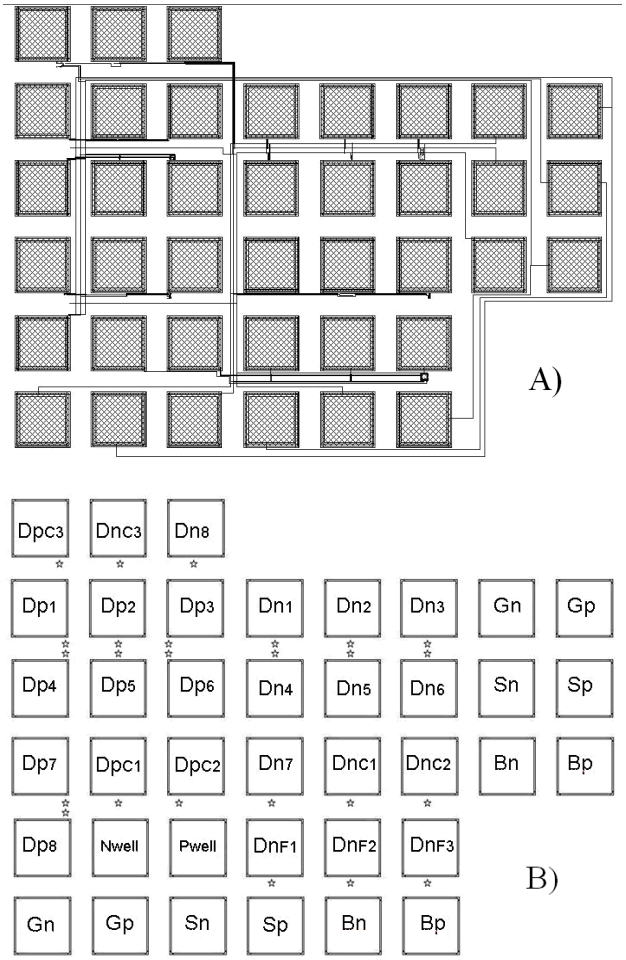


Figure 2 – (A) Micro-pads layout and (B) Micropads configuration and transistor location.

Several test structures was designed in order to applicable to all operation regions and all device sizes. The test structures inside the test chip include long (L = 10µm), short (L = 0.18µm), wide (W = 10µm) and narrow (W = 0.22µm) channel transistors. Other geometries are also presented, such as series-parallel associations of transistors (TAT's) of different sizes and shapes [4].

These structures are used to characterize the behavior of the drain current, gate transconductance, output conductance, noise and intrinsic frequency in terms of geometry, association of unit transistors and layout strategies. The test structures are measured by means of microprobes, so we used micro-pads to access the structures terminals (the PAD's, which were obtained from the IBM 0.18 µm technology library).

The chip microphotography, as shown in figure 1, has a total area (including 64 pads) of 6.8 mm². Most of the chip area is occupied by micro-pads, in order to access the device terminals for measurements. The area of each block is shown in table 1.

Figure 2a shows the micro-pads layout prototyped and figure 2b presents the micro-pads configuration and transistor location in order to access the structure terminals for testing and measurements. The test chip was fabricated containing a few equivalent composite transistors formed by different associations in 0.18µm CMOS technology composed by unit transistors of equal size. These associations and a reference transistor (a single transistor showing the same W/L relation as a functional reference) are used to achieve by comparative measuring the analog behavior [5]. Figure 3a shows an electrical composition of the prototyped TAT associations and the figure 3b the PMOS and NMOS TAT layout example.

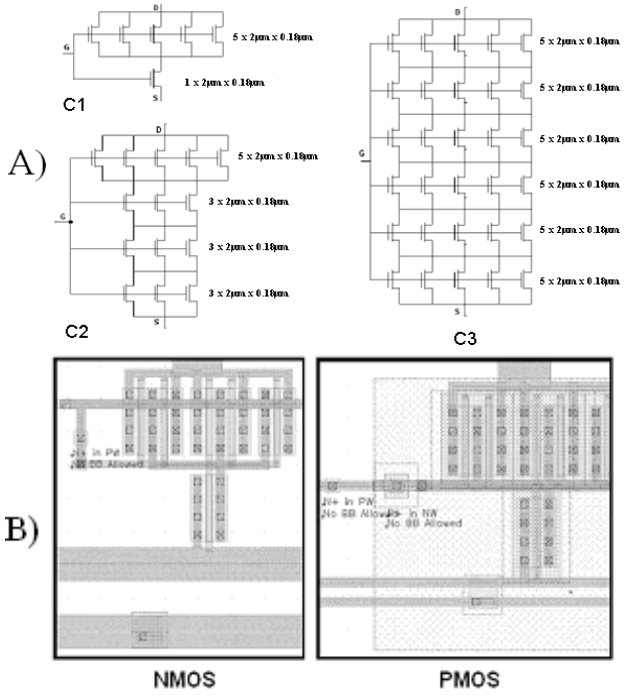
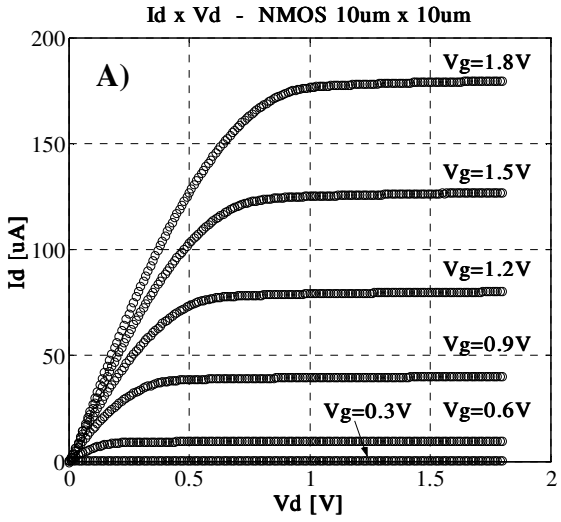


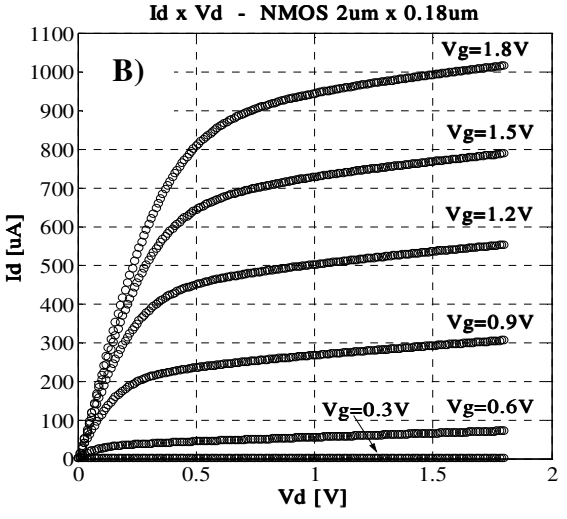
Figure 3 – (A) Electrical configuration of the prototyped TAT's and (B) NMOS and PMOS layout of C1 TAT.

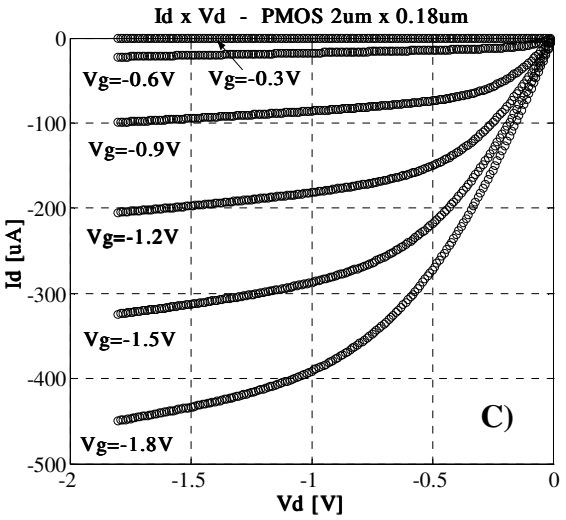
3. TEST CHARACTERIZATION PROCEDURE

The test and characterization procedure will follow two main steps. The first step is the characterization of the target process. Using a parameter analyzer and a microprobe station the basic DC measurements was obtained, such as Id x Vd and Id x Vg, under several bias conditions. Thus, many important parameters can be obtained.

Therefore, the process in use can be fully characterized and the parameters of CMOS simulation models (such as ACM and EKV models) can be obtained. This can be used to fine tune the basic design curves and validate the designed blocks performance. Drain current, gate transconductance, output conductance and noise can be obtained direct from the MOS transistors structures measurements. The maximum frequency for this target process can also be obtained, using the Ring Oscillator structure. Figure 4 shows some preliminary results for the MOS transistors characterization.







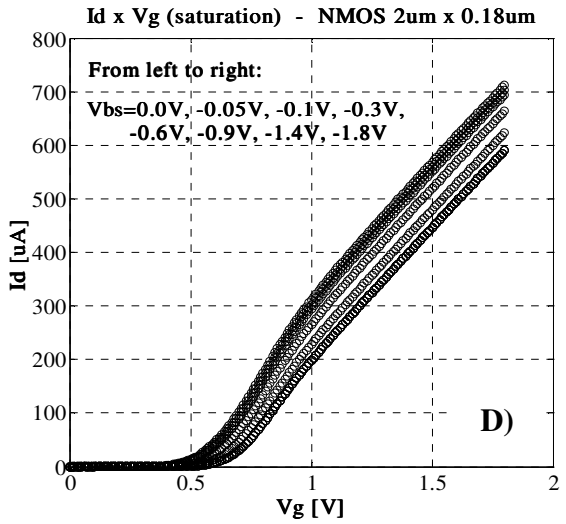


Figure 4 – (A) Id vs. Vd measured curves for a single NMOS Transistor 10µm x 10µm; (B) Id vs. Vd measured curves for a single NMOS Transistor 2µm x 0.18µm; (C) Id vs. Vd measured curves for a single PMOS Transistor 2µm x 0.18µm and (D) Id vs. Vg measured curves for a single NMOS Transistor 2µm x 0.18µm.

The Id x Vs characteristic is used to extract the parameter Vp (pinch-off voltage) of ACM model. This curve was obtained too, but it was not included in this paper.

The next step is the fully characterization and validation of each block. In order to verify the gate delay for this process, a ring oscillator was designed and characterized. To verify the resulting average delay time a 19 stage ring oscillator circuit was implemented. The final layout is presented in the figure 5 and the transistor sizes in the ring oscillator are Wp = 0.6µm, Wn = 0.4µm and Ln = Lp = 0.18µm.

We measured at a typical power supply voltage (± 1.8V) the oscillation frequency at about of 630 MHz, resulting in an average gate delay of 41.8ps.

Figure 6a illustrates the oscillation frequency dependency of the power supply and figure 6b the average delay versus supply voltage. These results were obtained using a spectrum analyzer through measurement of five samples.

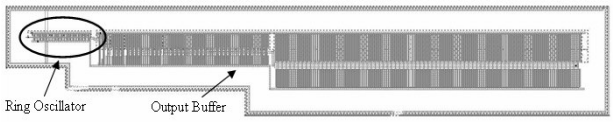


Figure 5 – Ring Oscillator final layout.

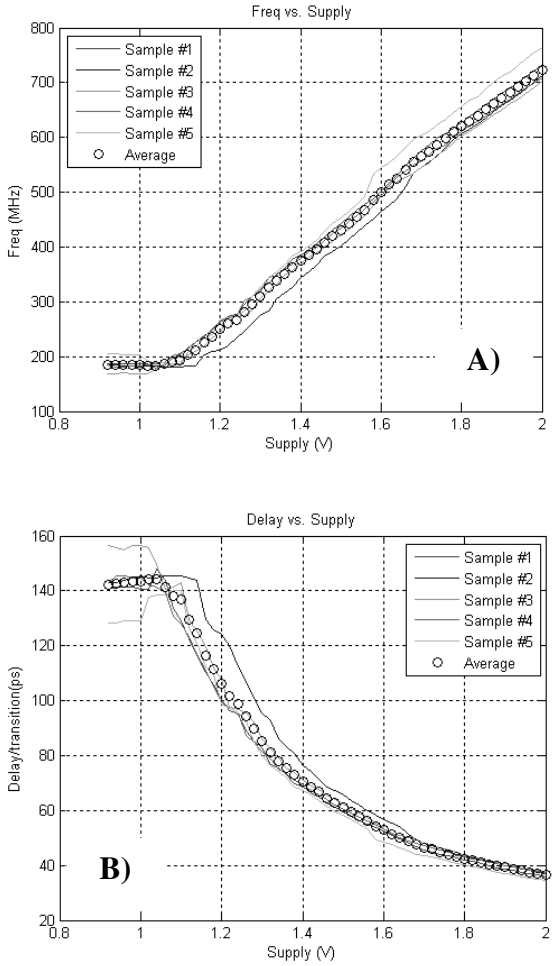


Figure 6 – Ring Oscillator results: (A) Frequency vs. Supply Voltage and (B) Delay vs. Supply Voltage.

4. CONCLUSIONS AND FUTURE WORK

Electrical characterizations based on measurements are fundamental for the complete analysis of an analog integrated circuit. Only measurements can determine the real circuit functionality. The prototyped test chip is currently under testing, and preliminary measurements of the designed blocks and test vehicles were presented, showing good results performance. As future work, we intend to perform a fully characterization and modeling optimization through electrical measurements to fine tune the basic design curves and validate the blocks performance.

5. ACKNOWLEDGEMENTS

The support of FAURGS, FINEP, CNPq and CAPES Brazilian agencies with scholarships and PDI-TI Program grant are gratefully acknowledged.

6. REFERENCES

[1] F.P. Cortes, E. Fabris and S. Bampi. Applying the gm/ID Method in the Analysis and Design of a Miller Amplifier, a Comparator and a Gm-C Band-Pass Filter. IFIP VLSI Soc 2003, Darmstadt, Germany, December 2003.

[2] F.P. Cortes and S. Bampi. Analysis, Design and Implementation of Baseband and RF Blocks Suitable for a Multi-Band Analog Interface for CMOS SOCs. PHD Thesis, PGMICRO – UFRGS, Porto Alegre, Brasil, 2008.

[3] L. S. de Paula, E. Fabris and S. Bampi. A High Swing Low Power CMOS Differential Voltage-Controlled Ring Oscillator. In: 14th IEEE International Conference on Electronics, Circuits and Systems – ICECS 2007, Marrakech, Morocco, December, 2007.

[4] A. Girardi and S. Bampi. LIT - An Automatic Layout Generation Tool for Trapezoidal Association of Transistors for Basic Analog Building Blocks. In: Design, Automation and Test in Europe 2003 - DATE'03, Munich, Germany, March 2003.

[5] A. Girardi, F. P. Cortes and S. Bampi. Analog IC Modules Design Using Trapezoidal Association of MOS Transistors in 0.35µm Technology. In: 16th Symposium on Integrated Circuits and Systems Design (CHIP IN SAMPA), SBCCI 2003 Proceedings, São Paulo, Brazil, pp. 311-316, September 2003.