SINGLE-ELECTRON CONTENT-ADDRESS MEMORY CIRCUIT

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ABSTRACT

In this paper a content-address memory circuit fully implemented using single-electron tunneling devices (SET) is proposed and implemented. The memory circuit is based on SET flip-flops and a SET winner-take-all neural network. The SET content-address memory is validated by simulation and the operating temperature range is evaluated.

1. INTRODUCTION

Single-electron devices (SET) may become an extremely attractive option for the development of giga (GSI) and even tera (TSI) scaled integrated circuits. However, these devices are quite sensitive to environmental conditions (their behavior is strongly dependent on node impedances and on temperature and electromagnetic interference, as well as on offset charges and co-tunneling events). Several measures can be taken to minimize or to overcome these nuisances and they were taken into account in this work. This type of study is essential to evaluate the possibility of building complex single-electron device networks.

Many circuits using SET devices have already been proposed. Some of these proposals only replace CMOS devices for SET devices. Nevertheless, there are two critical points in this kind of strategy. The first one is that the operation of SET circuits is not deterministic, the major mechanism of charge transport is tunneling, which is a probabilistic phenomenon. The second one is random background charges which may degrade the operation of the circuit. To overcome these limitations, one strategy is to build new circuit architectures.

In previous works, circuit SET memories have already been proposed [1]. However, in this paper, a proposal of a system for implementing a content-address memory using single-electron basic circuits is presented.

2. PROPOSED CIRCUIT

A content-address memory circuit will be proposed and implemented based on SET flip-flops memories [2] and a SET winner-take-all neural network [3]. The SET memory circuit designed here is derived from a MOS circuit proposed in [4]. The block diagram of the proposed SET circuit is showed in Figure 1.

In each SET flip-flop memory circuit, according to the combination of set and reset inputs a different value is stored in Qi. When the control terminal b is high, this stored value can be read in the memory's output. When it is low, the memory's output is zero [2].

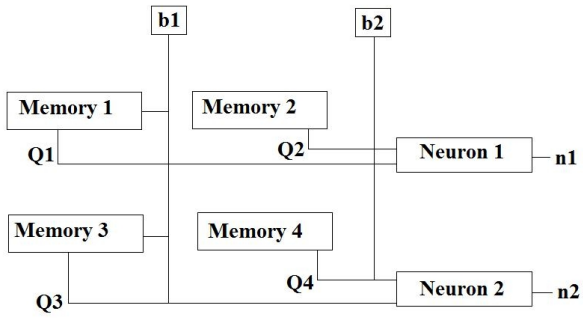

Fig.1: Block diagram of the proposed SET circuit.

In the modified SET-WTA circuit [5] the input SET transistor converts the input voltage to an output current. The neuron with the highest input current will be the winner, i.e., will have the highest output voltage and will inhibit its neighbors.

The proposed circuit is showed in Figure 2. The whole circuit will operate depending on control terminals b1 and b2 (see Figure 1). They can never be high simultaneously. When b1 is high, Q1 and Q3 can be read and will be comparated by the WTA network. In this case, the WTA network will work as a an exclusive-or gate, i.e., everytime Q1=Q3 the outputs of neuron 1 (n1) and neuron 2 (n2) are zero. Otherwise, when b2 is high Q2 and Q4 can be read and compared by the WTA network. The behavior of the proposed circuit is described in Table 1.

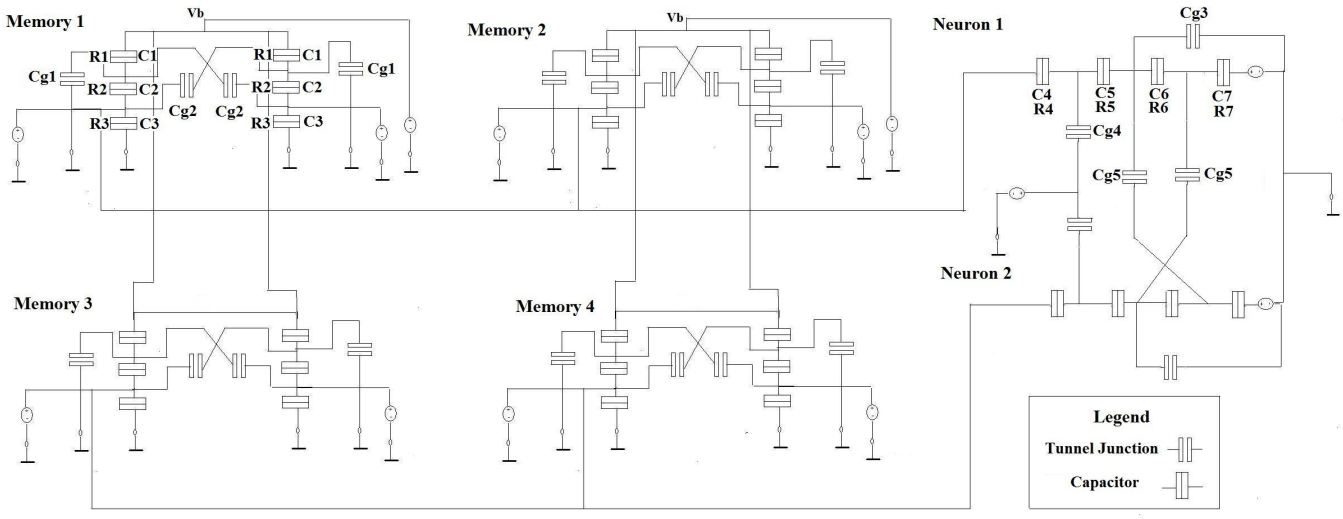

Fig.2: Proposed SET content-address memory circuit.

Table 1 – SET content-address memory circuit inputs and outputs

Control inputs		Memory outputs				Neuron outputs	
b1	b2	Q1	Q2	Q3	Q4	n1	n2
1	0	0	X	0	X	0	0
1	0	0	X	1	X	0	1
1	0	1	X	0	X	1	0
1	0	1	X	1	X	0	0
0	1	X	0	X	0	0	0
0	1	X	0	X	1	0	1
0	1	X	1	X	0	1	0
0	1	X	1	X	1	0	0

3. RESULTS

The performance of the proposed circuit was evaluated using the nanoelectronic simulator SIMON (*Simulation of nano-structures*) [6]. For the SET flip-flop memory circuit control voltages b1 and b2 where set to 0.048 V at logic level 1 and -0.048 V at logic level 0. This value and the others were obtained from [2].

For the SET WTA modified circuit capacitance, resistance and voltage values were directly obtained from [5]. All the values used on the devices of the proposed circuit are shown in Table 2. Consider that all memories are identical. The neurons are identical too.

In the simulations the input voltages were set to lowest possible value, in order to obtain the tunneling of one single electron at each time in the whole circuit. Taking that into account set and reset inputs were adjusted as square waves varying from zero to 0.076 V. Set and reset input voltages of memories 1 and 2 were equal. Their voltage waveform is shown in Figure 3. In the same way, reset inputs of both memories were also the same. Their waveform were adjusted to be exactly the opposite of their set inputs, i.e., whether set is high, reset is low and vice-versa. On the other hand, memories 3 and 4 will have the same inputs waveform in Figure 3 for their reset inputs.

Table 2 – Proposed SET content-address memory circuit values according to Fig. 2.

Devices	Values
R1=R2=R3	400 kΩ
R4=R5=R6=R7	1 MΩ
C1=C2=C3	1 aF
C4=C5	0.1 aF
C6=C7	0.01 aF
Cg1	1 aF
Cg2	3 aF
Cg3	100 aF
Cg4=Cg5	0.1 aF

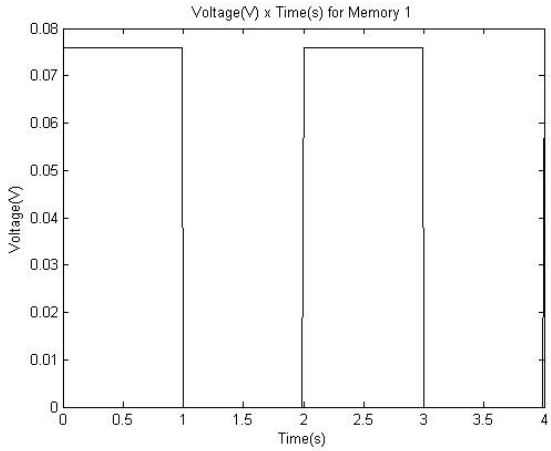

Fig.3:Set input for memories 1 and 2.

Control gates b1 and b2 waveforms are shown in Figure 4. It can be noted that b1 and b2 were never high at the same time, as said before.

The output voltages of neurons 1 and 2 are shown in Figure 5.

It can be observed in Figure 5 that the output voltages responded as desired to the input voltage variation, according to Table 1.The noise seen was originated from the operating temperature used in the simulation, which was 30K.

The operating temperature was increased up to 30 K and the circuit kept its funcionalities. For higher temperatures the circuit did not provide the desired output.

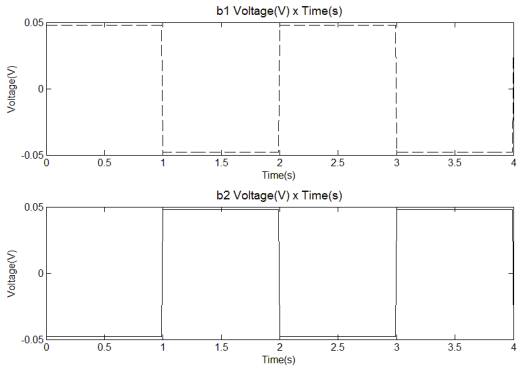

Fig.4: Control terminals b1 and b2 voltages

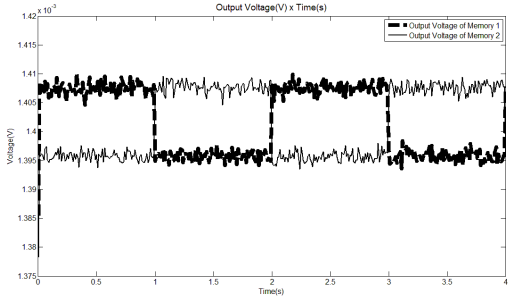

Fig.5: Output voltages of neurons 1 and 2 for T=30K.

The adaptability of content-address memory circuit is its major advantage. For different inputs is possible to apply the same architecture without any change in the circuit configuration.

4. CONCLUSIONS

In this paper a content-address memory fully implement using single-electron devices was proposed. The circuit was based on SET flip-flop memory circuits and SET WTA circuits.

The performance of the proposed circuit was sucessfully validated by simulation using SIMON

In the future the complexity of the proposed circuit will be increased to provide solutions for single-electron circuit applications. Furthermore, robustness against background charges and temperature will be enhaced to reach room temperature operation.

ACKNOWLEDGEMENTS

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