RADIATION EFFECTS ON FLIP-FLOP SOI CMOS

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ABSTRACT

This work presents a deep analysis of a D Flip-flop, composed by ten SOI MOSFET transistors, focusing on its static behavior as well as its susceptibility to radiation exposure. After the electrical characterization and the suitable extraction of parameters, especially the ones related to the individual threshold voltages, the circuit was simulated, confirming the model fidelity to the experimental results. Keeping the clock input constant while the D input voltage was varied, it was possible to study the outstanding Kink Effect influence on the Flip-flop outputs. Meanwhile, varying the clock input with a constant D input, it was interesting to notice how the transmission gates remarkably contributed to increase the output noise margins. Finally, the circuit was simulated under three different doses of radiation and the transition voltage variation was compared for the both cases previously mentioned, resulting in a 0.27 V change when the clock is constant and in a 0.32 V variation when D input is set to high logic level.

1. INTRODUCTION

The SOI ("Silicon-On-Insulator") MOSFET technology has been increasingly used during the past few decades, especially because of the very important advantages provided by its structure due to the presence of a buried oxide layer under the thin silicon film [1]. Besides the great potential to be used in integrated circuits, these components are much more convenient in harsh environments, in which low sensitivity to temperature variation [2] and high hardness against transient radiation effects are required [3], such as in the aerospace field.

This mentioned remarkable radiation hardness is essentially caused by the effect of the buried oxide layer, which isolates the active region of this kind of transistor, reducing or even eliminating undesirable effects caused by events such as single-event upset, single-event latchup and many others [4].

In order to carefully investigate how SOI MOSFET technology behaves in harsh environments from a comprehensive point of view, a D Flip-flop circuit was studied. This device was chosen since it is composed by both pMOS and nMOS transistors, associated as inverters and transmission gates. Besides that, this component may be interpreted as a primitive memory cell with a 1-bit storage capacity, consisting a basic element widely used in many electronic devices.

The goal of this work is to study the static behavior and the radiation influence on SOI D Flip-flops up to 100 krad.

2. DEVICES CHARACTERIZATION AND SIMULATIONS

The SOI MOSFETs used in this work were fabricated with 1 μm SOI CMOS technology in the Interuniversity MicroElectronics Centre (IMEC), Belgium. This technology uses 20, 400 and 180 nm of gate oxide, buried oxide and silicon film thickness, respectively. The partially depleted (PD) SOI nMOSFET transistors are enhancement-mode, while the fully depleted (FD) SOI pMOSFET ones are accumulation-mode. The channel length (L) is 1 μm for the transistors used in the inverters and 2 μm for the ones used in the transmission gates. All of them have a 20 μm channel width (W).

In order to simulate the radiation effects in a D Flip-flop circuit, the AIM SPICE with the BSIM3 SOI model was used. The parameters inserted in the performed simulations were experimentally obtained for each transistor, even the individual threshold voltage (V_{th}), extracted based on the second derivative method [5].

3. FLIP-FLOP CIRCUIT

After the mentioned transistors characterizations, these devices were connected as it is shown in Figure 1, resulting in a D Flip-Flop, with its two inputs (D and Clock) and two outputs (Q and Q').

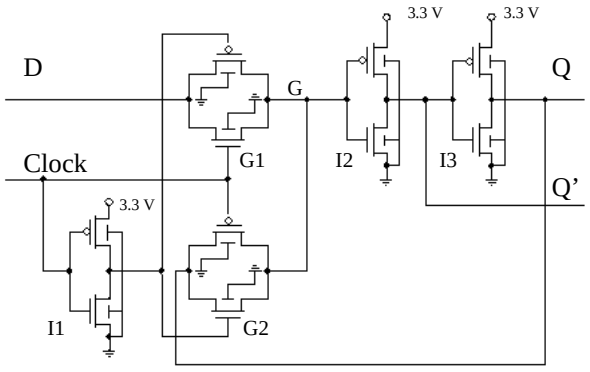

Figure 1 – D Flip-flop circuit with SOI MOSFETs

In brief, the analyzed D Flip-flop is composed by three inverter circuits and two transmission gates. Firstly, when the clock input is "1", the transmission gate connected to the D input (G1) is kept enabled while the one connected to the Q output (G2) remains unable. In

this situation, Q output presents the same logic level of D input, as it is expected from a level-sensitive D flip-flop. Exactly the opposite occurs with the transmission gates when the clock input is "0". In other words, only G2 is kept enable, preventing Q output from changing its logic level. The two last inverter (I2 and I3), meanwhile, contribute to avoid the degradation of the two studied outputs.

In order to study the circuit static behavior, two different kinds of analyses will be performed. At first, the clock input will be set as "1", while the Q and the Q' outputs will be examined in function of D input value. In the second case, it will be studied the transference curve as the clock input raises, with Q previously set to "0" and D in constant high level.

4. STATIC ANALYSIS

Before the radiation influence study, the procedure for both mentioned kinds of analyses will be composed of a comparison between the experimental data, obtained with the Agilent 4156C semiconductor parameters analyzer, and the simulated results, taking the individual extracted parameters into consideration.

In the first case, the results obtained for Q and Q' outputs voltages in function of D input value is presented in Figure 2.

First of all, it is noticeable that the simulated results may be considered very close to the experimental ones, confirming the reliability of the transistors simulated model and, consequently, its suitability to the circuit conditions.

Besides that, it is possible to extract from the graph the transition voltages (V_{INV}) for this first case, which is approximately 1.7 V for both Q and Q' outputs. Regarding the noise margins, it is clear that they are bigger in the Q output curves, as an expectable result of inverters series combination.

Moreover, one of the most interesting characteristic presented by Figure 2, is related to the Kink Effect and its influence in the transference curve format, remarkably different from the standard one.

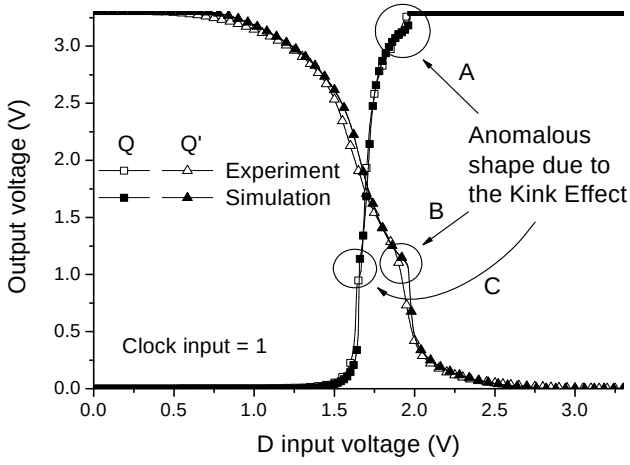

Figure 2 - Experimental and simulated output voltages versus D input voltage.

In order to explain this particular occurrence, it is essential to bear in mind how each output is related to the circuit inverters and transmission gates. Since during this analysis the clock input is set to constant high logic level, there will not be any transition in I1 inverter, meanwhile the G1 transmission gate will always be enabled and the G2 transmission gate will be permanently unable. Therefore, the Q output transference curve format depends mostly on the I2 and I3 inverters features at the same time as the Q' output curve depends basically on I2 characteristics.

These dependence relations are exactly the reason why the Q output curve presents the Kink Effect abrupt influence twice (points A and C), meanwhile the Q' output presents it only once (point B). Subsequent to a careful analysis, it is possible to conclude that the I2 nMOS transistor is in the Kink Effect region only when the D input voltage is lower than 1.95 V (A and B) and the I3 one is influenced by the Kink Effect when the input voltage is higher than 1.65 V (C).

The Kink Effect impact on the transference curves may be clearly understood by graphically comparing the simulated results with and without this effect parameters, how it is displayed in Figure 3.

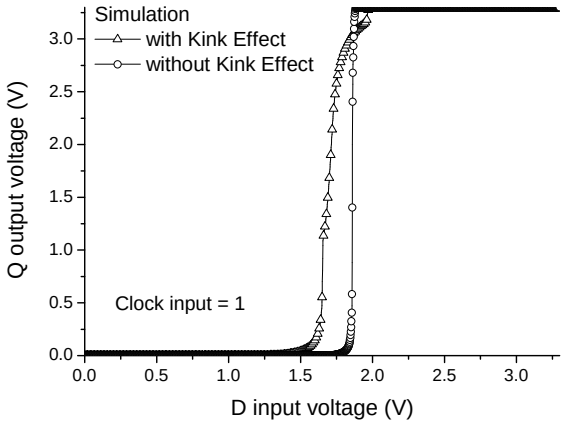

Figure 3 - Q output voltage versus D input voltage with and without Kink Effect parameters.

In the second case, the experimental and the simulated Q output data as a function of the clock input voltage are exhibited in Figure 4.

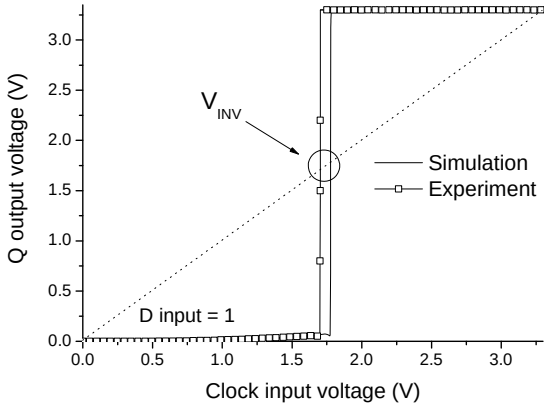

Figure 4 - Experimental and simulated output voltages versus Clock input voltage.

Once more, the difference between the transition voltage in the analyzed curves was less than 0.1 V, reaffirming the simulated model suitability. The Q output logic state changed when the clock input voltage was 1.70 V according to the experimental curve, very close to 1.77 V suggested by the simulated one.

Comparing Figures 2 and 4, the most noticeable difference is related to the abrupt logic state commutation in the second case or, in other words, to the bigger noise margins when the D input is constant.

In order to investigate this phenomenon, it is important to compare the G-node voltage variation in both cases, as it is shown in Figure 5.

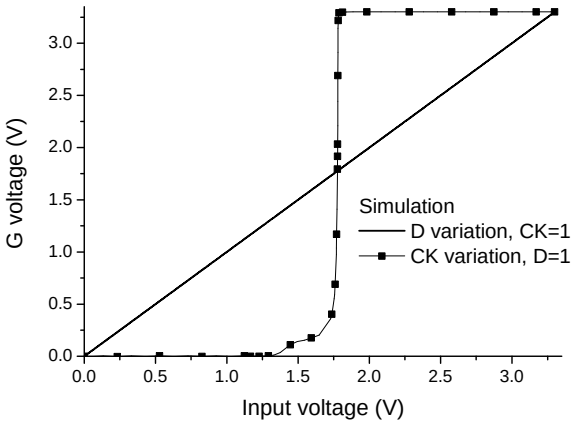

Figure 5 - Transmission gate output voltage (G voltage) versus input voltage for D and Clock variation.

In the first case, since the clock input is constantly in high logic level, the G1 transmission gate is kept enabled at the same time as G2 is unable. As a result, D input value is directly transmitted to G node, ensuing in its linear format.

On the other hand, as the clock input increases in the second case, G1 equivalent resistance tends to decrease while G2 resistance raises. Consequently, G node voltage gradually begins to increase as soon as G1 pMOS transistor is turned on. Afterwards, when the G node voltage is big enough to trigger Q output logic state commutation; both the transmission gates inputs are set to high logic level. Finally, G node voltage abruptly reaches the power supply voltage, bringing about the peculiar format revealed by Figure 5.

Once the G node is the input for the I2 and I3 inverters series combination, it expectable, indeed, that the noise margins tend to be much bigger in the second case (Figure 4) than in the first one (Figure 2).

5. RADIATION INFLUENCE

After the analysis of the Flip-flop static behavior, the circuit was simulated under different doses of radiation. The radiation effect was modeled considering the threshold voltage variation as the most significant impact, as it is shown in Table 1.

The V_{th} parameter for each transistor was calculated using the experimentally obtained individual threshold voltage under no radiation and its variations due to radiation influence extracted from reference [6]. According to the mentioned data resource, devices were irradiated with ^{60}Co exposures doses of 0, 10, 50 and 100 krad, after a 5 krad/hour dose-rate.

Table 1 – Threshold voltage shift after radiation [6]

Dose (krad)	ΔV_{th}: nMOS (V)	ΔV_{th}: pMOS (V)
10	-0.01	-0.20
50	-0.10	-0.45
100	-0.20	-0.55

Subsequently, the previously performed simulations were repeated for each radiation exposure dose, once more making use of AIM SPICE. The obtained results for the first case, with the clock input constant, are presented in Figure 6.

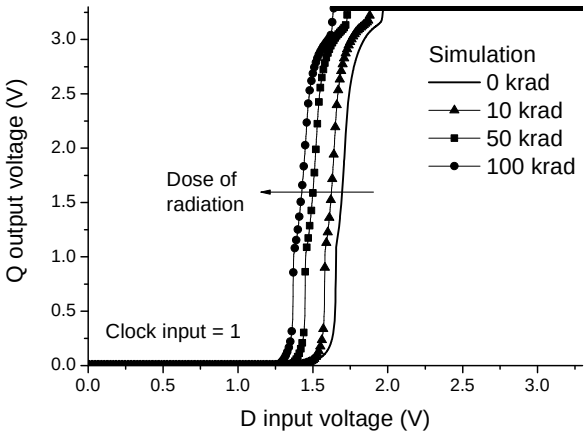

Figure 6 - Q output voltage versus D input voltage for different doses of radiation.

Analyzing the plotted curves, it is clear that the transition voltage declines as the radiation dose raises.

In order to examine this phenomenon, it is important to notice that D input voltage is directly transmitted to the G node, exactly the same way it happens without radiation exposure. Therefore, the transference curve variation depends mostly on I2 and I3 parameters susceptibility to radiation effects.

Since buried oxide charges increase due to the radiation impact, it is expected that V_{th} declines for pMOS and nMOS transistors, as it is suggested by Table 1. Accordingly, the low noise margin decreases and the high noise margin increases. In other words, the inverters transition voltage tends to decline, as detailed explained in [7].

As a result, Q' output logic level commutation occurs for a smaller D input voltage and, consequently, Q output state is induced to change as well. Finally, it is possible to take from the graph that, under 100 krad radiation dose, the transition voltage declines 0.27 V.

Following the same methodology, the obtained data in the second case, with constant D input, are exhibited in Figure 7.

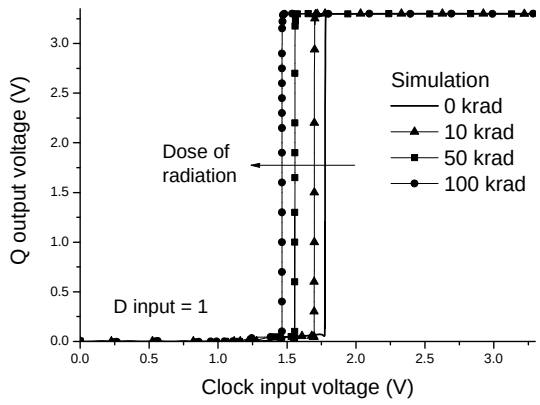

Figure 7 - Q output voltage versus clock input voltage for different doses of radiation.

Once more, it is evident that in the second case the transition voltage declines as the radiation dose increases.

On the other hand, differently from the previous case, the transmission gates and the I1 inverter play the major role in the radiation influence on the static transference curve.

Carefully analyzing the Flip-flop circuit represented in Figure 1, it is possible to conclude that, as the I1 transition voltage decreases under radiation exposure, G1 transmission gate becomes enabled for a lower clock input voltage, at the same time as G2 becomes unable. Hence, G-node voltage abruptly increases for a lower input voltage and, consequently, the Flip-flop state changes as well.

Regarding quantitative alterations, Figure 7 shows that, under 100 krad radiation dose, the global transition voltage declines 0.32 V.

A comparison of the transition voltage variation in both cases is displayed in Figure 8.

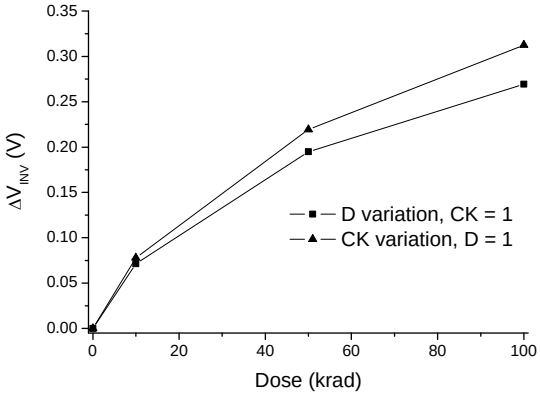

Figure 8 - Transition voltage variation versus dose of radiation for D and Clock variation.

Initially, Figure 8 shows that the transition voltage variation is more relevant in the second case, when D input is constant.

This remarkable behavior may be explained based on the G-node voltage dependence on radiation impact. As previously mentioned, although in the first case the G-node voltage does not suffer any interference, in the second one it is unmistakably affected by I1 susceptibility to radiation exposure and its consequence on G1 and G2 performance.

Since I2 and I3 influence is the same for both cases, it is expectable, indeed, that the transition voltage variation tends to be more notorious when the D input is constant as much as 19% under 100 krad exposure.

As a final observation, it is important to notice that even in the worst case, the transition voltage variation was less than 10% of the supply voltage, reaffirming SOI technology suitability in harsh environments.

6. CONCLUSION

In this work, an SOI Flip-Flop was studied, highlighting its static transference curve in function of D and Clock input variation separately.

According to the experimental data, it was concluded that the Q output logical commutation occurs when variable input voltage is 1.7 V for both cases. Regarding the curves format, there is no doubt that the Kink Effect is exceptionally significant, resulting in an anomalous transition when the clock input is constant. On the other hand, when D input is constant, the noise margins outstandingly increase, which may be put down to the transmission gates influence.

Modeling the radiation influence based on the individual threshold voltages variation, it was concluded that the transition voltage decreases up to 0.27 V when the clock input is kept constant and almost 20% more for the second case, due to the I1 inverter influence on the transmission gates behavior.

As a whole, the current project laid emphasis on an SOI Flip-Flop static behavior from a global point of view, reassuring its appropriateness in a glittering array of technological applications.

7. ACKNOWLEDGEMENTS

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8. REFERENCES

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