HIGH FREQUENCY CAPACITANCE VERSUS VOLTAGE CURVES ANALYSIS IN PI-GATE SOI MOSFET STRUCTURES

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ABSTRACT

This paper shows the aspects of the gate-to-substrate capacitance versus gate voltage curves of a Pi-Gate SOI MOSFET. The curves were obtained from two dimensional numerical simulation of the gate to substrate capacitance at high frequency. The influence of the depth of the gate extension in the oxide and the channel width reduction were analyzed. A better comprehension of the Pi-gate capacitance behavior is present. The capacitance curve shows a higher dependence with the channel width reduction and with the increase of the gate extension depth.

1. INTRODUCTION

During the last years, the dimensions of the transistors are being drastically reduced. However this miniaturization is reaching its limits and can be slowed down. To overcome this problem new materials and architectures are being studied .

New structures, such as multiple-gate silicon-on-insulator MOSFETS, have been proposed due to their ability to overcome several limitations like low speed and reduced short-channel effects (SCEs) [1]. The most important types of multiple-gate SOI MOSFET devices are summarized in Figure 1, represented by the number of gates around the channel.

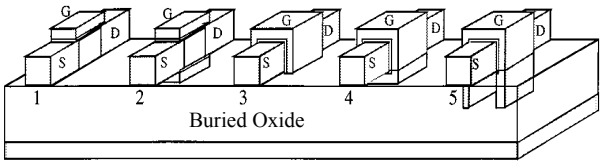


Figure 1 – Single-gate(1), double-gate(2), triple-gate(3), quadruple-gate (4) and Pi-gate SOI MOSFET(5)[1].

Of all SOI MOSFET structures, triple-gate transistors are very promising because it combines good subthreshold characteristics with high on-currents and are considered to be very good alternatives to planar devices in the sub 50 nm gate-length [2]. Improved versions of triple-gate SOI MOSFETS are being studied. For instance, the Pi-gate has great potential to replace the current used devices do to its geometry that is part-way between triple-gate and quadruple gate devices [3,4]. The gate goes down into the buried oxide, allowing a more effective control of the electrostatics in the channel region and shielding it from the electric-field lines originated in the drain when the width of the devices is small enough [5,6]. Figure 2 presents the Pi-Gate SOI MOSFET structure, representing its important geometrical parameters: the gate length (L), fin width (W_{fin}), fin height (H_{fin}), depth of the gate extension into the oxide (d_{ext}) and the buried oxide thickness (t_{oxb}).

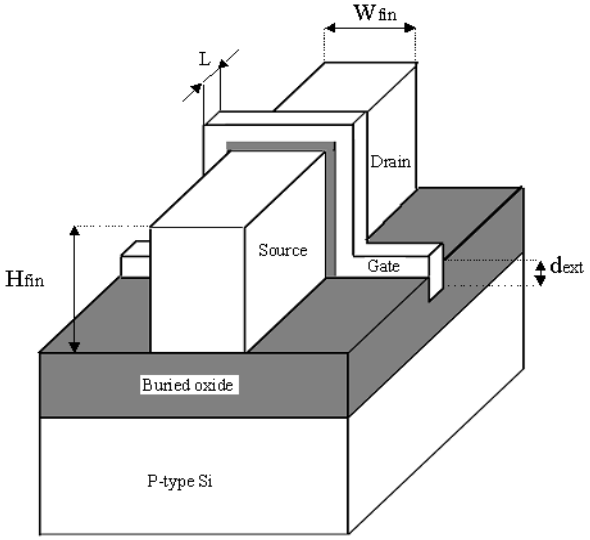


Figure 2 – Pi-Gate SOI MOSFET structure.

Curves of the capacitance in function of the gate voltage (C-V) are well known as a good tool for parameters extraction of planar devices. Although, this new structure that is being studied, present a different capacitance behavior from the conventional, mainly when small channel width dimensions (narrow-fin) are used.

In this work we studied the effective capacitance in narrow-fin devices vs. quasi-planar (very wide-fin) devices using C-V simulations for a better understanding of Pi-gate SOI MOSFET behavior. Some notable characteristics of gate-to-substrate capacitance behavior in Pi-gate SOI MOSFETs are discussed varying the

depths of the extension of the gate electrode into the buried oxide.

2. DEVICES STRUCTURES

A schematic cross section of the Pi-Gate SOI MOSFET is shown in Figure 3, representing the capacitors present in these structures: the capacitance between the front gate and the channels (C_{oxf}), the capacitance between the front and back silicon interfaces (C_{Si}), the capacitance between sidewall channel and the bottom silicon interface (C_L), the capacitance between the back gate and the back interface (C_{oxb1}) and, for last, C_{oxb2} and C_{oxb3} the capacitances between the extension of the front gate in the buried oxide and the back gate. These last are due to the presence of three gates around the channel and the extension depth of the gate into the buried oxide.

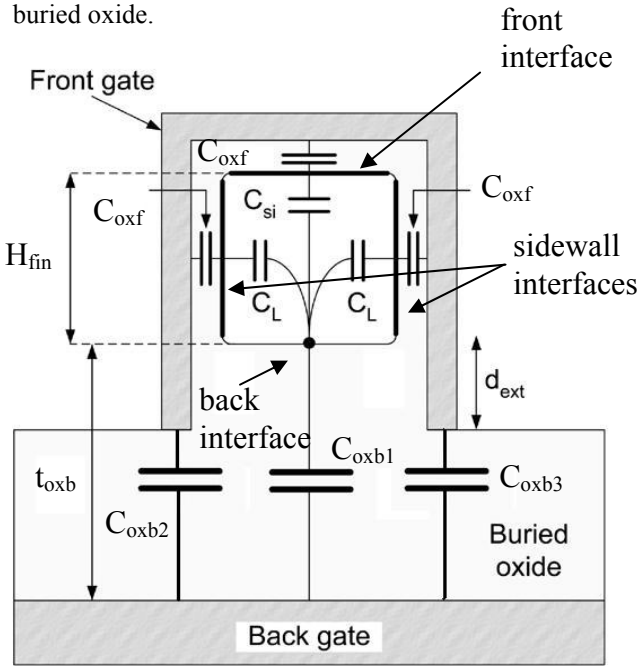


Figure 3 - Pi-Gate SOI MOSFET cross section showing the capacitors presents in this structures.

3. NUMERICAL SIMULATIONS

The device's electrical characteristics were simulated using the Device2D Atlas software package from Silvaco. Curves of the gate to substrate capacitance as a function of the front gate voltage (C-V) were simulated at high frequency f=1MHz.

The Pi-Gate SOI MOSFET structures were simulated with the following parameters: channel length L=1 μm, W_{fin}=120nm, TiN gate material with work function ϕ_M = 4.7 eV, effective oxide thickness EOT=2 nm, buried oxide thickness t_{oxb}=145 nm, fin height H_{fin}=60 nm, channel doping concentration of $N_a=1x10^{15}$ cm^{-3} and several depths of the gate extension into the oxide d_{ext}=0, 20, 40, 60, 80nm e 120nm.

The channel of 1μm was chosen so that the effects between drain and source, like short channel effects, could be ignored in our analyses.

Figure 4 shows the gate to substrate capacitance as a function of the front gate voltage curves for different depths of the gate extension into the oxide (d_{ext}) and channel width of W_{fin}=120nm. It is possible to observe, that the maximum capacitance ($V_{GF} < 0$) increase as the depth of the gate extension is increased. The minimum capacitance ($V_{GF} > 0$) also presents an increase but it is smaller.

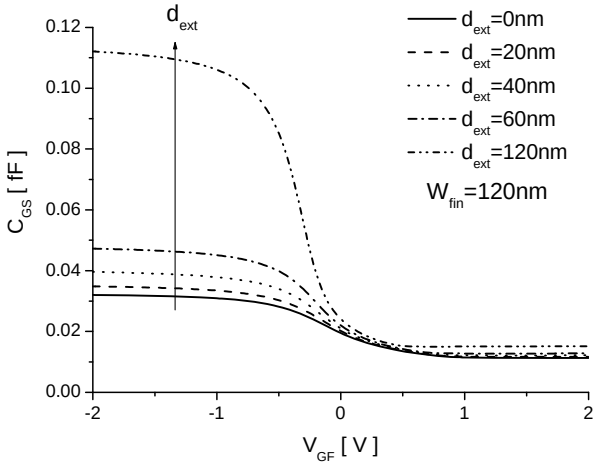
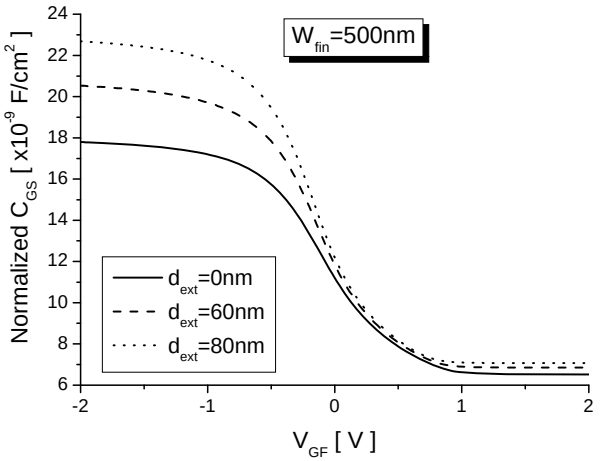


Figure 4 – Simulated gate to substrate capacitance as a function of the front gate voltage curves for different depths of the gate extension into the oxide d_{ext} and W_{fin}=120nm.

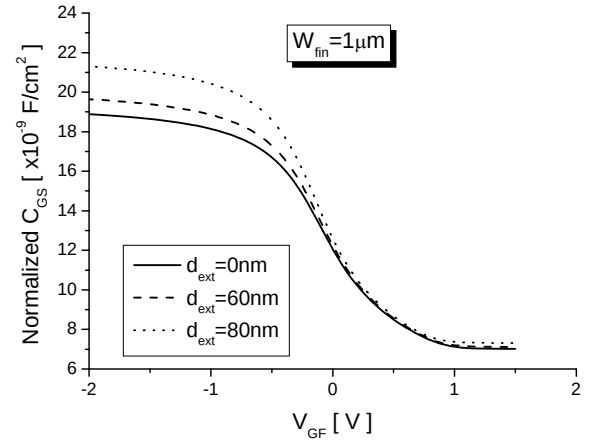
4. DEPENDENCE OF C-V CURVE WITH DEVICE PARAMETERS

Different channel widths were considered in order to study its influence on the C-V curves, varying the depths of the extension of the gate electrode into the buried oxide.

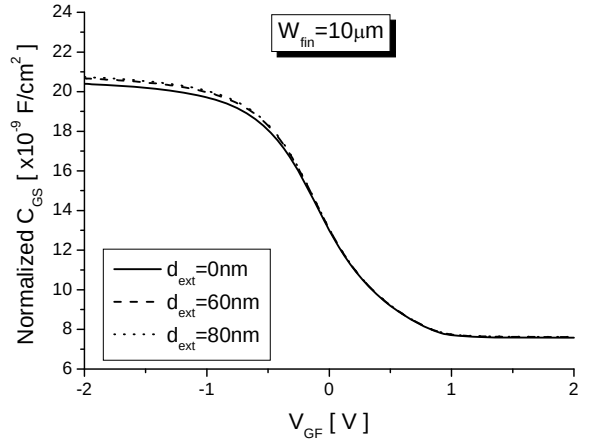
Figure 5 presents the normalized gate-to-substrate capacitance (C_{GS}) per unit gate area as a function of the front gate voltage curves for different depths of the gate extension (d_{ext}): a) W_{fin}=500nm, b) W_{fin}=1μm and c) W_{fin}=10μm. For narrow-fin the increase in maximum capacitance is more pronounced and as the channel width is increased this variation tends to disappear. The reason for that is that narrow width presents a higher coupling between the lateral gates.



(A)



(B)



(C)

Figure 5 – Simulated normalized gate-to-substrate capacitance as a function of the front gate voltage curves for different depths of the gate extension into the oxide d_{ext} and a) W_{fin}=500nm, b) W_{fin}=1μm and c) W_{fin}=10μm.

One can notice the existence of two variations in C_{GS} characteristics of narrow-fin devices in comparison with wide-fin devices. First, the low maximum capacitance observed in narrow-fin devices, while for W=500nm the capacitance is approximately 18nF/cm^2, for W=10μm the capacitance is more than 20nF/cm^2. Secondly, a higher variation of the maximum capacitance with higher gate extension depth for narrow-fin devices.

This variation in the maximum gate to substrate capacitance, normalized by $C_{GSmáx}$ extracted in the device with W_{fin}=10μm (considered as a planar device, where the associations of capacitances did not present variation), in function of the channel width can be observed in Figure 6, for different depths of the extension of the gate electrode into the buried oxide. Devices with wide-fin presented a lower variation in the maximum capacitance. Although, a decrease in it capacitance is observed for devices with narrow-fin except for a higher extension d_{ext}=120nm, where an increase is observed in $C_{GSmáx}$ as the channel width is increased.

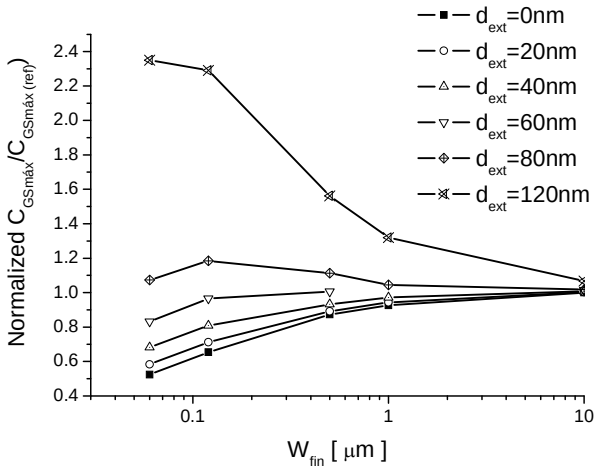


Figure 6 – Maximum capacitance variation in function of the channel width for different depth of the gate extension.

For a narrow-fin with high depth extension, the region underneath the silicon island is at a potential close to V_{GF}. So a virtual field-induce back gate is created. In wide-fin devices, the distance between the two gate extensions is too great for this effect to occur, and the bottom of the silicon island is not controlled by the gate potential.

Previous works described the capacitance lowering to be an effect of higher lateral gate coupling typical of multiple gate structures with narrow-fin. This coupling combined with ultra-thin gate dielectrics (with EOT=2nm) can result in very low effective capacitance [7].

Figure 7 presents the electric field distribution in the structure for channel width of 500nm and 120nm, depth extension of d_{ext}=80nm and a gate voltage of V_{GF}=-2V (accumulation in the channel). In both devices an electric field induced by the extension of the gate into the buried oxide is observed. Although, a more intense electric field and interactions from all fields generated is observed in narrow-fin devices (Figure 6B).

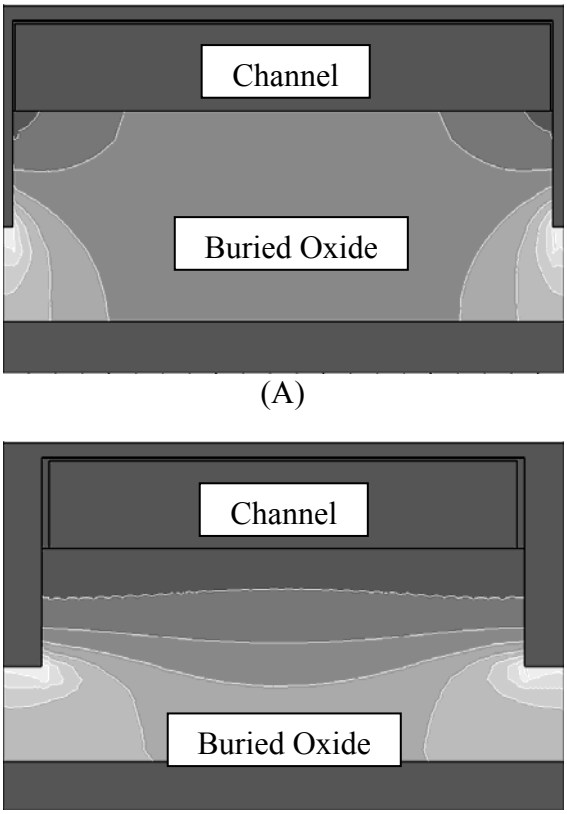


Figure 7 – Simulated electric field distribution created by the lateral gates of a device with d_{ext}=80nm, V_{GF}=-2V and different channel width a) W_{fin}=500nm and b)W_{fin}=120.

This increase in the maximum capacitance (C_{GS}) for high depth extension of the gate can be a result of this electric field that is more intense for narrow-fin devices, as observed in Figure 7.

5. CONCLUSION

In this paper, an analysis of gate to substrate capacitance versus front gate voltage curves (C-V) of Pi-gate SOI MOSFET devices was presented. The influence of the channel width reduction and of the depth of the gate extension in the oxide was verified through 2D numerical simulations.

A reduction in the maximum capacitance was observed with channel width reducing due to the higher lateral gate coupling, typical of multiple gate structures with narrow-fin.

On the other hand an increase in the maximum capacitance occurred with higher depth of the gate extension in the oxide. This variation in the maximum capacitance with the depth extension of the gate is more pronounced for narrow-fin devices where the lateral gates induce a higher electric field.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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