IMPROVED METHOD TO EXTRACT THE PARASITIC S/D RESISTANCE IN MULTIPLE-GATE FETS

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ABSTRACT

This paper proposes an improved method to extract the parasitic source/drain series resistance of FinFETs. It is an extension of a well-known method but takes also into account the channel resistance for application in a large range of channel lengths. Analytical and 3- D numerical simulations are used to test the proposed method. This method is applied experimentally in a Triple-gate FinFETs and the results are coherent with the technology used.

1. INTRODUCTION

Due to downscaling the planar MOSFET is reaching practical limits, regarding channel lengths below 50 nm. The use of complex transistor channel engineering is necessary in order to reach adequate threshold voltage and to reduce short channel effects but it causes mobility degradation, increases the sub-threshold swing and the parasitic junction capacitances [1]. In order to reach better short-channel characteristics Silicon-on-Insulator (SOI) technology has emerged to overcome the problems of bulk (conventional) MOSFETs [2]. The SOI Multiple-Gate (MuGFETs) has emerged in order to overcome the single gate SOI MOSFET limitations [3]. However, the source/drain series resistance can be high due to the presence of very thin dimensions of source and drain. In order to minimize this problem silicide is used in these regions [4].

There are different methods used to extract source and drain series resistance. Reference [5] presents an algorithm based on the resistance measurement technique to extract effective channel length and source/drain series resistance for planar MOSFETs indicating that both are gate-voltage dependent and is applicable to both conventional and LDD (Lightly Doped Drain) planar MOSFETs. The most commonly used model in planar conventional MOSFET is indicated in reference [6]. These two methods are inappropriate for FinFETs due to the three dimensional architecture of these devices. These methods are limited in terms of their ability to capture the series resistance issues arising from the narrow width of source and drain regions and current conduction on planes (perpendicular to the source and drain contacts). Reference [7] describes an extraction method of the parasitic source and drain resistance (R_{DS}) by using an analytical model, where a first-order exponentional curve fitting on the experimental data of the total resistance (R_{TOTAL}) as a function of gate to source voltage (V_{GS}) curve, generates an asymptotic part for high values of V_{GS}, the channel resistance (R_{CH}) diminishes asymptotically and R_{TOTAL} becomes equal to R_{DS}. However, for long channel devices the R_{CH} cannot be neglected anymore.

An example of FinFET is shown in figure 1, where H_{FIN} and W_{FIN} are fin height and fin width, respectively, and L is the channel length.

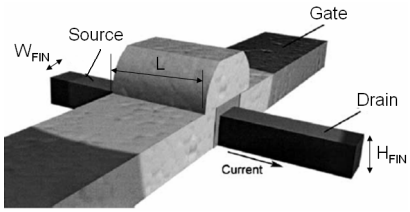

Fig. 1. Triple-Gate FinFET structure.

The goal of this work is to develop an improved extraction method of parasitic source/drain series resistance of FinFETs, valid for a large range of channel length and for different fin widths and heights. This extraction method takes into account the channel resistance. Analytical and 3-D numerical simulations are used in order to test the proposed method. This improved method is also applied experimentally.

2. PROPOSED METHOD

In the proposed method is necessary to measure I_{DS}xV_{GS} curves at low V_{DS} value, using at least two FinFETs with different channel lengths. Higher accuracy is reached if more than two devices are used. Based on I_{DS}xV_{GS} curve, it is possible to calculate the total resistance (channel and source/drain resistances) by dividing V_{DS} over I_{DS} and plotting an R_{TOTAL}xL curve for a fixed value of V_{GS}. The total resistance can be written according equation (1).

$$R_{TOTAL} = \frac{V_{DS}}{I_{DS}} = R_{CH} + R_{SD} \quad (1)$$

Where:

$$R_{TOTAL} = f\left(\frac{L}{W_{FIN} \cdot H_{FIN}}\right) R_{CH} = f\left(\frac{L}{W_{FIN} \cdot H_{FIN}}\right) R_{SD} = f\left(\frac{1}{W_{FIN} \cdot H_{FIN}}\right)$$

The equation (1) shows that total and channel resistances are dependent on channel length while parasitic source/drain series resistance is not.

Considering that in Multiple-Gate technology the lateral diffusion from source/drain to channel is negligible [7], if a linear regression of R_{TOTAL}xL is performed, the R_{DS} can be obtained by getting the value of the resistance where L is equal to zero, where R_{CH}=0. The V_{GS} has to be large enough (V_{GS}>>V_{TH}) in order to have the transistor working in the linear region.

The Figure 2 presents the R_{TOTAL} as a function of channel length where R_{SD} is presented.

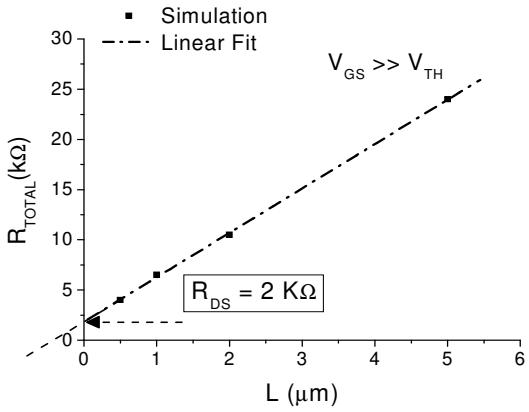

Fig. 2. R_{TOTAL} as a function of channel length.

The results can be considered trustable when the correlation coefficient of the linear regression is higher than 0.9999.

3. SIMULATION RESULTS

3.1. Analytical Simulations

Analytical simulations are performed in order to verify the independence of the source and drain series resistance on the channel length for different gate to source voltages. Figure 3 shows the circuit used to perform the analytical simulations to obtain I_{DS}xV_{GS} curves for four different channel lengths (0.5, 1, 2 and 5 micrometers) and for three different W_{FINs} (60, 120 and 500 nm), considering V_{DS} equal to 25 mV and source and drain series resistances equals to 1 KΩ. The total resistance of source and drain (R_{SD}), in this case, is equal to 2 KΩ. In this simulation is considered the following parameters: p-type doping concentration (N_A) equal to $1x10^{15}$ cm^{-3}, gate-oxide (t_{ox}) and buried oxide (t_{box}) thickness equals to 2 nm and 145 nm, respectively.

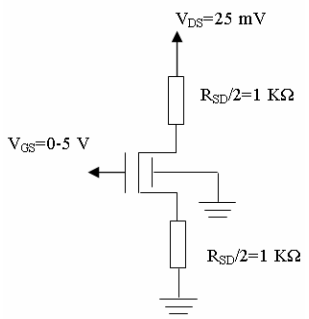

Fig. 3. Circuit used to produce I_{DS}xV_{GS} curve.

Figure 4 shows the R_{TOTAL} x L for different gate voltages, by applying the proposed method in the I_{DS}xV_{GS} curves.

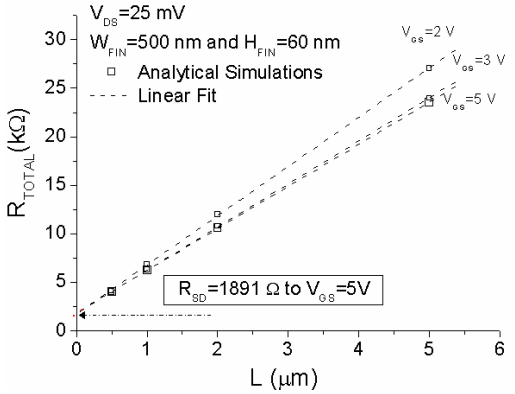

Fig. 4. R_{TOTAL} as a function of channel length for four different gates voltages obtained by analytical simulations.

Figure 4 shows that, increasing channel length also increase R_{TOTAL} as expected. This means that R_{CH} cannot be neglected and is therefore incorporated into the R_{TOTAL} value. Besides, the extracted R_{TOTAL} values also vary as a function of V_{GS} for different channel lengths. However, the extracted R_{SD} has shown to be independent on the applied V_{GS}, indicating that smaller gate voltages can be used for the extraction of this parameter. This is particularly interesting for state-of-the-art transistors in which the thin gate oxide limits the allowed bias voltage (typically < 1.5 V). Additionally, all of the extracted R_{TOTAL} values, for each V_{GS} considered, can be perfectly adjusted by linear fit (Linear Adjust Coefficient around 99.99 %). Table I presents the R_{SD} values extracted from Figure 4 by applying this simple method.

Table I. R_{SD} as a function of V_{GS} values, the linear adjusted coefficient and the error.

Source/Drain Series Resistance (Ω)			
V_{GS} (V)	**R_{SD} (Ω)**	**Linear Adjust Coefficient**	**Error (%)**
5	***1891***	***0.99998***	***5.5***
4	1871	0,99997	6.5
3	1832	0.99996	8.4
2	1732	0.99992	13.4

Table I shows that, the value of extracted R_{SD}, becomes nearest to the defined value of source/drain series resistance (R_{SD}=2 KΩ) for the highest V_{GS} value, in this case, equal to 5 V. This means that the extracted R_{SD} (1891 Ω, for V_{GS}=5 V) using this simple method presents an error of around 5.5 % from the real value. Even reducing V_{GS} the error is not very significant.

Applying the extraction method of source/drain series resistance which neglects the channel resistance [7], using the same data of simulations presented before is presented in Table II.

Table II. R_{SD} as a function of V_{GS} values based on method where R_{CH} is neglected [7]. R_{SD}=2 kΩ in the simulation.

L (μm)	**R_{SD} [Ω] (V_{GS}=5V)**	**R_{SD} [Ω] (Proposed Method)**
0.5	3990	1891
1	6254	1891
2	10603	1891
5	23517	1891

It can be seen by analyzing Table II that the extracted source/drain series resistance varies as a function of channel length, which is unreal, and the method proposed in ref [7] can not be applied for these transistors channel lengths. This means that the influence of R_{CH} in the R_{SD} can not be neglected. In the same way, these two extraction methods of source/drain series resistance were applied on I_{DS}xV_{GS} curves generated by three dimensional numerical simulations [8].

For four different channel lengths (0.5, 1, 2 and 5 micrometers) and for three different W_{FINs} (60, 120 and 500 nm), considering V_{DS} equal to 25 mV.

3.2. Three-Dimensional Numerical Simulation.

The triple-gate FinFETs structures were done by using DevEdit3D from TCAD (Silvaco) [8]. In this simulation the parameters were set as follow: p-type doping concentration (N_A) equal to $1x10^{15}$ cm^{-3}, gate-oxide (t_{ox}) and buried oxide (t_{box}) thickness equals to 2 nm and 145 nm, respectively.

The parameters of LDD region were: n-type doping concentration (N_{LDD}) equal to $1x10^{20}$ cm^{-3}, LDD length (L_{LDD}) equal to 50 nm, source and drain length ($L_{S/D}$) equal to 50 nm.

Figure 5 present the extracted source and drain series resistance as a function of channel length for different fin widths.

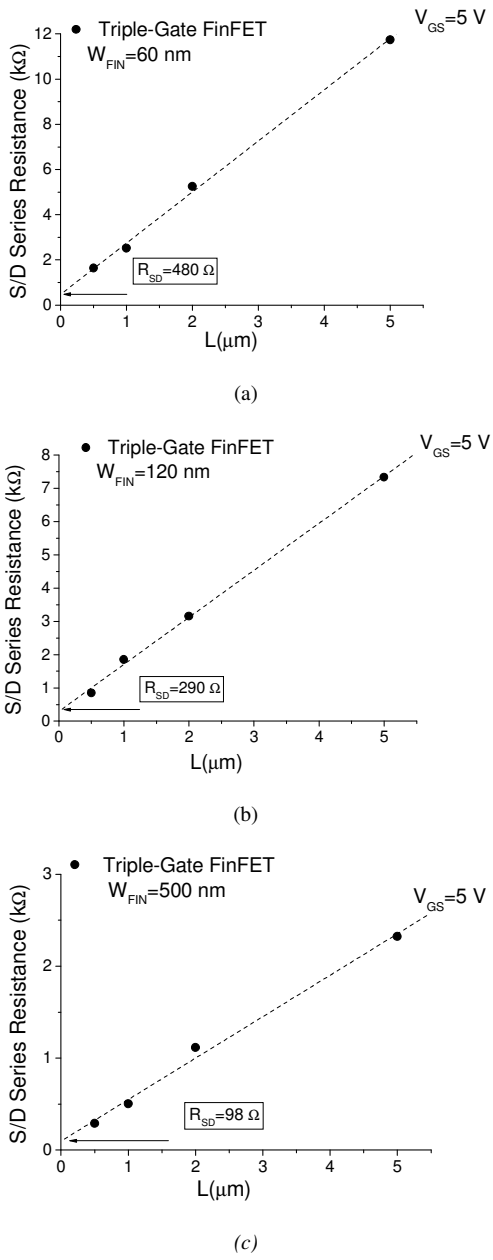

Fig. 5. Source and drain series resistance as a function of channel length for different W_{FIN} [(a): 60 nm, (b): 120 nm and (c): 500 nm] and gate voltage (5 V).

Figure 5 demonstrated that the proposed method is dependent on the channel length for different fin widths in contrast to the method that does not takes into account channel resistance. Figure 6 shows the extracted source and drain series resistance as a function of fin width for different channel lengths.

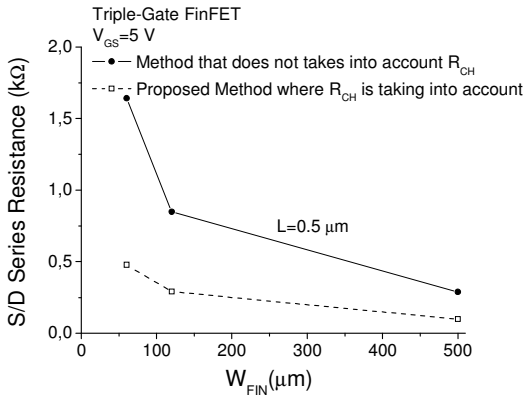

Fig. 6. Source and drain series resistance as a function of fin width for different channel lengths, with V_{GS}=5 V.

Note in figure 6 that nonplanar devices suffer from a high parasitic source/drain resistance due to the narrow width of their source/drain region, or increasing the fin width, the source/drain series resistance diminishes.

4. EXPERIMENTAL RESULTS

The proposed method was also applied on triple-gate FinFETs with thirty multiple fingers, fabricated at IMEC/Belgium in order to perform the electrical characterization of source and drain series resistance for eight different channel lengths. The characteristics of these devices were: p-type doping concentration (N_A) equal to $1x10^{15}$ cm^{-3}, fin height (H_{FIN}) equal to 60 nm, fin width (W_{FIN}) equal to 20 nm, gate-oxide (t_{ox}) and buried oxide (t_{box}) thickness equals to 2 nm and 145 nm, respectively. The parameters of LLD region were: source and drain n-type doping concentration ($N_{S/D}$) equal to $1x10^{21}$ cm^{-3}, LDD length (L_{LDD}) equal to 50 nm, source and drain length ($L_{S/D}$) equal to 50 nm and V_{DS} equal to 50mV. Figure 7 present the extracted source and drain series resistance as a function of channel length for different gate voltage.

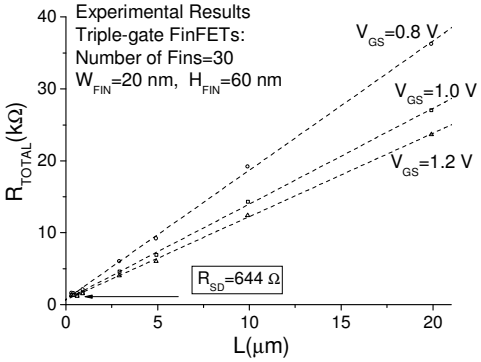

Fig. 7. Source and drain series resistance as a function of fin lengths for different channel lengths, with different V_{GS}.

Table IV presents the extracted values of series resistance of the presented curves in Figure 7, for different values of gate voltage.

Table IV. R_{SD} as a function of L, based on the proposed method.

V_{GS} (V)	R_{SD} (Ω)	Linear Adjust Coefficient
0.8	725	0,9996
1.0	676	0,9996
1.2	***644***	***0,9996***

Observing Table IV, the source/drain series resistance extracted value tends to 644 Ω, considering the highest value of V_{GS}, which in this case is equal to 1.2 V.

5. CONCLUSIONS

A well-known method of source/drain series resistance of FinFETs, is improved in order to be used also for long channel length, taking in consideration the channel resistance.

The proposed method needs two or more devices with similar source/drain series resistance but with different transistors channel lengths. We tested the method using analytical and 3-D numerical simulation for transistors from 0.5 to 5 μm and an error lower than 5.0% is obtained. The proposed method was applied experimentally in a triple-gate FinFET and the results are coherent with the technology used.

6. REFERENCES

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