A SIMPLE MODEL TO ESTIMATE INTRINSIC POWER CONSUMPTION IN CMOS LOGIC GATES

[1]E. J. D. Chiappetta Filho, [1]P. F. Butzen, [1]L. S. da Rosa Jr., [2]A. I. Reis, [1]R. P. Ribas

[1]Instituto de Informática – UFRGS, Porto Alegre, Brazil
[2]Nangate Inc., Sunnyvale, CA, USA
{ejdcfilho, pbutzen, leomarjr, rpribas}@inf.ufrgs.br, are@nangate.com

ABSTRACT

Dynamic power dissipation is one of the most critical parameters in CMOS digital circuits design. In this work, a fast method to estimate the intrinsic power consumption, based on transistor capacitance model, is proposed. Experimental results have been carried out, and good correlation with SPICE simulation was obtained.

1. INTRODUCTION

Power dissipation is no longer a secondary issue in CMOS digital design [1]. The increasing complexity and high-performance requirements of modern integrated circuits have led to high power consumption.

Transistor level simulators with continuous-time modeling of the devices, like SPICE, can be very expensive in terms of storage and computation time. Hence, a great effort has been devoted in the development of accurate analytical expressions power models [2-4].

Traditional gate-level power estimations are based on the simplified assumption that the supply current required by a CMOS circuit is essentially spent in charging load capacitances at outputs of the switching gates [5]. These output capacitances are mainly composed by the input capacitances of next interconnected gates. However, intrinsic capacitances also contribute for the power dissipation and cannot be neglected in the cell power estimation analysis, being a significant element in the cell power estimation analysis.

In this context, the main goal of this work is to provide an analytical model to estimate intrinsic power consumption based on the charge required by intrinsic capacitances associated to a CMOS cell.

2. PROPOSED MODEL

The MOS capacitances can be divided in gate (C_G), depletion (C_{DB} and C_{DS}) and overlap (C_{GD} and C_{GS}) capacitances, as shown in Fig. 1a. In this work, a simplified model that considers only the intrinsic capacitance, illustrated in Fig. 1b, is used. The drain and source capacitances are defined as follow:

$$C_D = C_{DB} + C_{GD} \quad (1)$$

$$C_S = C_{SB} + C_{GS} \quad (2)$$

All capacitances are a linear function of the transistor width and can be modeled as follow:

$$C(w) = K\left(\frac{W}{W_{\min}} - 1\right) + C_{\min} \quad (3)$$

where, K is a constant value that modeling the transistor width dependence, W is the transistor width, W_{min} is the minimum transistor width and C_{min} is the capacitance for the minimum transistor width.

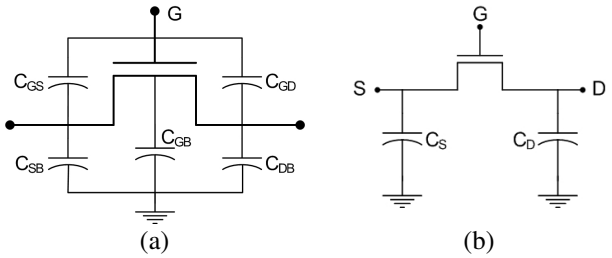

Figure 1 – Capacitance model: (a) MOSFET and (b) simplified approach.

Disregarding the process variability, the drain and source area can be considered the same and, consequently, $C_{DB} = C_{SB} = C_{DEP}$.

In the proposed analysis, MOS transistor is evaluated in cutoff and saturation regions. Linear region is ignored since it is a transitory state and it does not compromise the model accuracy. According to [6], C_{GD} is considered always zero and C_{GS} is $2/3*C_G$ in saturation mode.

Based on previous statement, the intrinsic capacitance can be modeled as shown in Table 1.

Table 1 – Intrinsic capacitances modeling.

Capacitance	Cutoff State	Saturation State
C_D	$C_{DEP}(w)$	$C_{DEP}(w)$
C_S	$C_{DEP}(w)$	$C_{DEP}(w) + 2/3*C_G(w)$

2.1. Parameter Extraction

The C_{DEP} parameters, K and C_{min}, for a NMOS transistor are extracted from electrical simulation using the structure depicted in Fig. 2a, while the structure illustrated in Fig. 2b is used to extract the C_G parameter.

Two simulations with different transistor width (W_{min} and $5*W_{min}$) are performed for each structure. The integral of the current value is measure, according equation (4), during the signal transition:

$$C(w) = \frac{1}{V_{dd}} \int_0^t i.dt \qquad (4)$$

These simulations provide two capacitance values, C_{min} and C_{5min} for two different transistor widths, W_{min} and W_{5min}, making possible modeling the capacitance according equation (3).

The C_{min} value is obtained directly from the W_{min} simulation. The K value is obtained from equation (5):

$$K = \left(\frac{C_{5\min} - C_{\min}}{4 * W_{\min}} \right) \qquad (5)$$

The PMOS parameters are extracted using similar procedure.

2.2. Capacitance Charged by Threshold Voltage

NMOS transistor is not good conductor of logic value '1', while the PMOS one is not good conductor of logic value '0'. In these cases, the intrinsic capacitances in the terminals of these transistors are already charged by the threshold voltage. To consider this charge in the final power consumption the capacitances are replaced by equation (7) and (8).

$$C_{D+Vth} = \left(\frac{V_{dd} - V_{th}}{V_{dd}} \right) C_D \qquad (7)$$

$$C_{S+Vth} = \left(\frac{V_{dd} - V_{th}}{V_{dd}} \right) C_S \qquad (8)$$

2.3. Case Study: Method Demonstration

To illustrate the procedure described in the previous sub-section, the gate depicted in Fig. 3 is used as example. Considering the initial input vector [a,b,c] = [0,1,1], the transition in input 'c' from '1' to '0' results in the estimated intrinsic capacitances describe in Table 2.

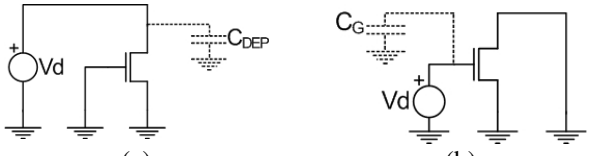

Figure 2 – Structure used to extract the parameters: (a) C_{DEP} and (b) C_G.

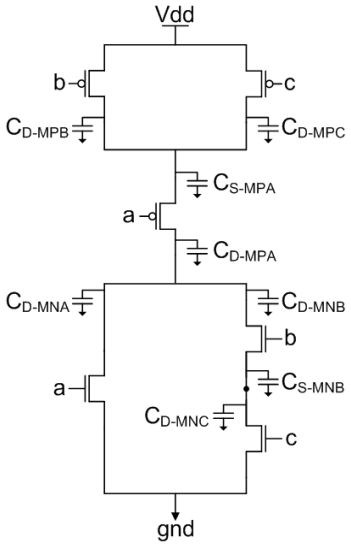

Figure 3 – AND-OR-INV (AOI) CMOS gate.

Table 2 – Intrinsic capacitances values for the logic gate depicted in Fig. 3.

Capacitance	Value
CD-MPB	$\left(\frac{V_{dd} - V_{th}}{V_{dd}} \right) C_{DEP\_P}(4w)$
CD-MPC	$\left(\frac{V_{dd} - V_{th}}{V_{dd}} \right) C_{DEP\_P}(4w)$
CS-MPA	$C_{DEP\_P}(4w) + \frac{2}{3} * C_{G\_P}(4w)$
CD-MPA	$\left(\frac{V_{dd} - V_{th}}{V_{dd}} \right) C_{DEP\_P}(4w)$
CD-MNA	$C_{DEP\_N}(w)$
CD-MNB	$C_{DEP\_N}(2w)$
CS-MNB	$\left(\frac{V_{dd} - V_{th}}{V_{dd}} \right) \left(C_{DEP\_N}(2w) + \frac{2}{3} * C_{G\_N}(2w) \right)$
CD-MNC	$\left(\frac{V_{dd} - V_{th}}{V_{dd}} \right) C_{DEP\_N}(2w)$

2.4. Power Consumption by Intrinsic Capacitances

The power dissipated by the intrinsic capacitances of a CMOS gate is the one used to charge them. The discharge current is supplied by the charge stored in the capacitances and should not be accounted in total power consumption.

Considering the previous statement, the power dissipated by the intrinsic capacitances is the one when the output changes from '0' to '1'. The total intrinsic power consumption of a CMOS gate for a specific transition in the input vector is given by equation (9).

$$P = \sum (C_i) * V_{dd}^2 \quad (9)$$

3. EXPERIMENTAL RESULTS

To validate the proposed method, the results obtained analytically were correlated with HSPICE simulation data, considering a standard 130nm CMOS process.

The logic gate presented in Fig. 3 was evaluated to all three input combinations when the output signal range from '0' to '1'. The results shown in Table 3 demonstrate a good correlation to HSPICE simulation data.

Table 3 – Intrinsic power estimation.

Input vector transition [a,b,c] → [a,b,c]	Proposed Model (fW)	HSPICE Value (fW)	Error (%)
[0,1,1] → [0,1,0]	7,02	7,85	10,6
[0,1,1] → [0,0,1]	5,98	6,90	13,3
[1,0,0] → [0,0,0]	2,69	3,11	13,5

4. CONCLUSIONS

In this work a fast method to estimate the intrinsic power consumption of CMOS logic gates was presented. The model is based on the analysis of the intrinsic capacitances of logic gates. The results demonstrated a good correlation with the SPICE simulation. As future works it is intended to include the load and the short-circuit power analysis to provide the total dynamic power estimative. The intrinsic and load capacitances are closely related to the logic cell delay. Thus, through the investigation of these components, a method for delay estimative may be easily obtained.

5. REFERENCES

[1] D. Liu and C. Svensson, "Power Consumption Estimation in CMOS VLSI Chips," *IEEE Journal of Solid State Circuits,* vol. 29, no.6, pp. 663 - 670, June 1994.

[2] F. Najm, "A survey of power estimation techniques in VLSI circuits" IEEE Trans. VLSI Syst., vol. 2, pp. 446–455, Dec. 1994.

[3] A. Bogliolo et al. "Gate-Level Power and Current Simulation of CMOS Integrated Circuits," *IEEE Transactions on VLSI Systems,* vol. 5, no.4, pp. 473 - 488, Dec. 1997.

[4] M. Alioto, "A Simple and Accurate Model of Input capacitance for Power Estimation in CMOS logic," *IEEE Int. Conf. on Electronics, Circuits and Systems,* pp. 431 – 434, Dec. 2007.

[5] C. Y. Tsui, M. Pedram, and A. Despain, "Efficient estimation of dynamic power dissipation under a real delay model," *IEEE Int. Conf. Computer-Aided Design*, pp. 224–228, 1993.

[6] J. P. Uyemura, *CMOS Logic Circuit Design*, Kluwer Academic Publishers, 1999.