TEMPERATURE INFLUENCE ON SOI CMOS DEVICES

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ABSTRACT

This work presents a careful study of the temperature influence on SOI MOSFET devices static behavior, taking into consideration nMOS and pMOS individual transistors and the logic inverter circuit. Based on the drain current graph as a function of drain and gate voltages, it was possible to evaluate the temperature impact on different relevant parameters, such as the threshold voltage and the mobility degradation. In order to widely understand the temperature impact, specific characteristics were studied, namely the Edge Transistor Effect on the SOI pMOS devices and the Kink Effect on the nMOS ones. The temperature influence on classic inverter characteristic parameters was emphasized, focusing on the transition voltage, the noise margins and the maximum voltage gain for different temperature values and channel length ratio configurations.

1. INTRODUCTION

The SOI ("Silicon-On-Insulator") MOSFET transistors are considered as the succeeding technology of digital and analog electronics. The structural advantages of these new devices in comparison with common bulk ones are mainly related to the presence of a buried oxide layer under the thin silicon film [1]. This configuration brings to these transistors not only the possibility of being used in integrated circuits, but also much better suitability under harsh environments, such as at extreme temperatures [2] and under radiation impact [3], which allows this technology to be used in a glittering array of applications, likewise the aerospace field.

The main reason for this previously mentioned temperature and radiation hardness is the isolation of the transistors active region due to the presence of the buried oxide layer. As a result, unwanted effects related to these exposures [4] can be reduced or even eliminated.

Therefore, nMOS and pMOS transistors and a logic inverter circuit combining these components were studied in order to scrutinize the SOI MOSFET behavior in harsh environments, in particular at extreme temperatures, which take place in some computers, spacecrafts and so on. In special, the CMOS inverter has a fundamental importance since it combines the two most primary devices in microelectronics, being widely used in both analog and digital circuits.

The goal of this work is to study the temperature influence on SOI nMOS and pMOS transistors and on a logic inverter circuit, comparing the devices behavior at room and low temperature.

2. DEVICES AND METHODOLOGY

The SOI MOSFET transistors used in the current work were fabricated with 1 μm SOI CMOS technology in the Interuniversity MicroElectronics Centre (IMEC), Belgium. This technology makes use of 20, 400 and 180 nm of gate oxide, buried oxide and silicon film thickness, respectively. The partially depleted (PD) SOI nMOSFET transistors are enhancement-mode, while the fully depleted (FD) SOI pMOSFET ones are accumulation-mode. The used transistors had a channel length of 1 and 3 μm for both SOI nMOS and pMOS devices, commonly identified as L_N and L_P, respectively. All of them have a 20 μm-wide channel (W).

In order to simulate the temperature influence on the SOI technology, the individual transistors were experimentally characterized, based on the curves of the drain current as a function of the gate voltage (I_D x V_{GS}) and the drain current as a function of the drain voltage (I_D x V_{DS}) not only at room temperature (300 K = 27 ºC) but also at liquid nitrogen temperature (77 K = -196 ºC). The low temperature condition was experimentally obtained by filling a recipient with boiling liquid nitrogen and the parameters extraction method followed the proposal of [5].

Finally, SOI nMOS and pMOS transistors were properly associated according to the classic inverter circuit topology and the static transference curve was experimentally obtained for two different configurations L_N/L_P, repeating the mentioned temperature study procedure.

3. TEMPERATURE IMPACT ON THE INDIVIDUAL TRANSISTORS

First of all, the temperature influence on the I_D x V_{GS} curve was studied, since it makes possible the analysis of some very relevant parameters modification, such as the threshold voltage (V_{th}) and the carriers mobility (μ).

The experimentally obtained results for SOI pMOS and nMOS transistors are exhibited in Figure 1.

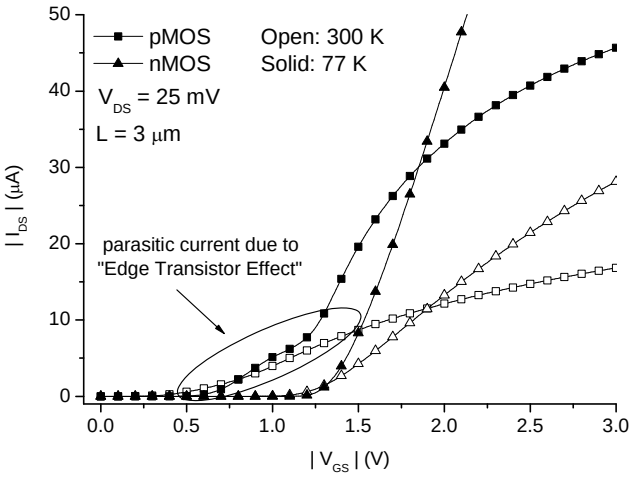

Figure 1 – Drain current as a function of the gate voltage for SOI nMOS and pMOS transistors at 77 and 300 K.

Based on the theoretical point of view of the widely know equation 1, which states a direct relation between the threshold voltage and the Fermi potential, it was expected an increase in the nMOS V_{th} at low temperature, because of the Fermi potential increment expressed by equation 2. Similarly, a | Vth | rise is expected for SOI pMOS transistors.

$$V_{th} = \Phi_{MS} + 2\Phi_F - \frac{Q_{OX}}{C_{OX}} - \frac{Q_{depl}}{C_{OX}} \qquad \text{(eq. 1)}$$

$$\Phi_F = \frac{KT}{q}\ln\left(\frac{N_a}{3{,}9.10^{16}T^{1.5}e^{-(E_g/2KT)}}\right) \qquad \text{(eq. 2)}$$

where V_{th} is the transistor threshold voltage [V], Φ_F is the Fermi potential [V], Φ_{MS} is the difference between metal and semiconductor work function [V], Q_{OX} is the oxide charge per unit area [C.cm^{-2}], Q_{depl} is the depletion region charge per unit area [C.cm^{-2}], C_{OX} is the oxide capacitance per unit area [F.cm^{-2}], K is the Boltzmann constant [eV.K^{-1}], q is the elementary charge [C], T is the temperature [K], N_a is the acceptable concentration [cm^{-3}] and E_g is the band gap energy [eV].

Analyzing the Figure 1, it is possible to notice, at a first glance, the increment of the maximum mobility, as it is theoretically expected at low temperature.

Regarding the threshold voltage, the nMOS curve shows, indeed, a slight enhancement and, accordingly, the zero temperature coefficient (ZTC) point appears when the drain current is independent on the device temperature. On the other hand, the pMOS curve is quite interesting, not only due to the more evident threshold voltage variation and ZTC point but also because of the remarkable shape in the highlighted area, which reveals an "edge transistor" effect coming into sight under very low temperature.

This noteworthy outcome, as well as the ZTC point, may be undoubtedly noticed by plotting the I_{DS} x V_{GS} curve with a logarithmic scale in the drain current axis, as it is displayed in Figure 2.

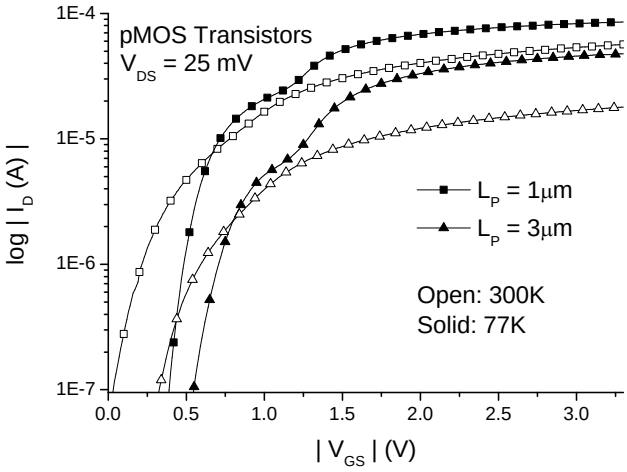

Figure 2 – Drain current as a function of the gate voltage for SOI pMOS transistors at 77 and 300 K.

The "edge transistor" effect is caused by the turn on current of an intrinsic parasitic transistor, as a consequence of the smaller carrier concentration near the edge of the structure than in the main transistor. Hence, this "edge transistor" threshold voltage, which is smaller than the main transistor one, dramatically changes the standard format of the I_D x V_{GS} logarithmic curve, as it is demonstrated by the experimental results presented in Figure 2.

The consequent presence of two peaks in the I_D x V_{GS} second derivative curve and the low temperature impact on its behavior can be deeply investigated based on the graph shown in Figure 3.

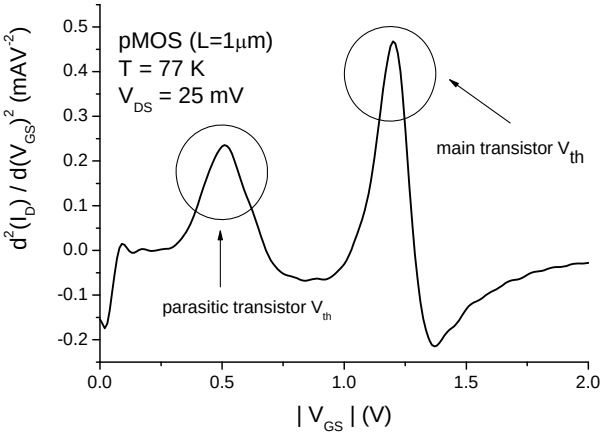

Figure 3 - I_D x V_{GS} second derivative as a function of the gate voltage for SOI pMOS transistor at 77 K.

The format of the curve presented in Figure 3 clearly reveals the major role that low temperature plays on the I_D x V_{GS} second derivative curve and, in other words, in a pMOS transistor threshold voltage. While at room

temperature there was a single peak, related to the main threshold voltage (0.88 V), at low temperature there are two clearly identifiable peaks, the first of which refers to the parasitic edge transistor (0.51 V) and the second one (1.20 V) is connected to the main threshold voltage shift.

Cautiously analyzing the I_D x V_{GS} curves for all the studied transistors, it was possible to evaluate the temperature influence by extracting the individual threshold voltages. The results obtained for L = 3 μm are summed up in Table 1.

Table 1 – Threshold voltage for pMOS and nMOS transistors with L = 3 μm at 77 and 300 K.

	V_{th} (300 K)	V_{th} (77 K)	
	main	edge	main
pMOS	-0.88 V	-0.70 V	-1.25 V
nMOS	1.24 V	1.33 V	

After focusing on the threshold voltage variation based on the I_D x V_{GS} curves, it is also important to examine the temperature impact on the I_D x V_{DS} graph. The results displayed in Figure 4 highlight the nMOS data, since it allows not only the study of the temperature impact, which is analogous for both nMOS and pMOS transistors, but also the observation of the Kink Effect, typical of partially depleted nMOS devices.

Noticeable under both low and high temperatures, the Kink Effect is originally caused by the migration of holes due to impact ionization and the consequent body potential increase when the drain voltage raises. Therefore, the threshold voltage decreases and the drain current tends to become more relevant, as it is easily seen in Figure 4 [6].

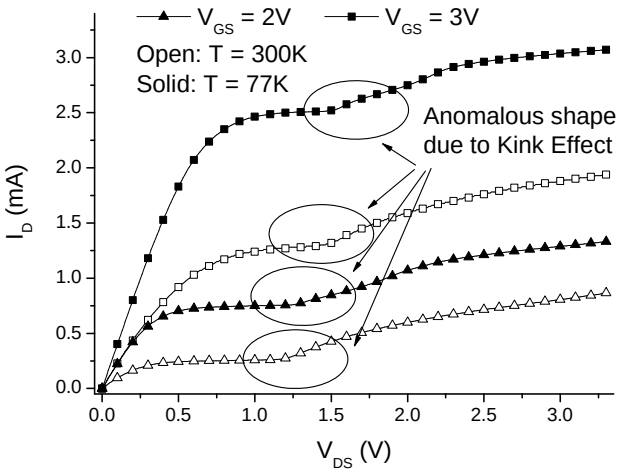

Figure 4 – Drain current as a function of the drain voltage for SOI nMOS transistors at 77 and 300 K.

Considering the mentioned data, it is possible to conclude that the most significant low temperature impact is indeed related to the increase of the drain current due to an expectable enhancement in the carriers mobility. The mobility degradation temperature factor (n) that determines the relation between the temperature variation and the carriers mobility ratio (equation 3) can be experimentally extracted. Taking into consideration the linear proportionality between the carriers mobility (μ) and the transconductance (g), which may be obtained from the I_D x V_{GS} derivative curve, it is possible to calculate the n values based on equation 4.

$$\frac{\mu_{T1}}{\mu_{T2}} = \left(\frac{T_2}{T_1}\right)^n \qquad \text{(equation 3)}$$

$$n = \frac{\log \frac{g_{\max T1}}{g_{\max T2}}}{\log \frac{T_2}{T_1}} \qquad \text{(equation 4)}$$

Considering the experimental values obtained for L = 3 μm, which are less susceptible to the short channel effect, the mobility degradation temperature factor value for SOI nMOS transistor was 1.01 and for pMOS one was 1.09. This result expresses a quasi-linear relation between the device temperature and its mobility inverse. Therefore, the clear increment in the drain current at low temperature observed in Figure 4 is once more justified due to the much more significant temperature impact on the mobility than on the threshold voltage.

4. TEMPERATURE IMPACT ON THE LOGIC INVERTER CIRCUIT

After the individual characterization, the SOI transistors were associated in order to compose the classic inverter circuit with two different channel length ratio (L_N/L_P) configurations.

The experimentally obtained static transference curves for the inverters at room and at low temperature are presented in Figure 5.

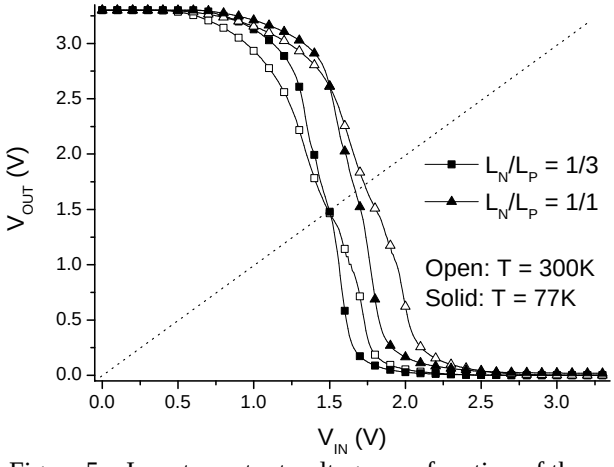

Figure 5 – Inverter output voltage as a function of the input voltage at 77 and 300 K.

Therefore, it is possible to extract very important inverters parameters, such as the transition voltage (V_{Tinv}), the low and high noise margins (NM_L and NM_H respectively) and the maximum voltage gain, based on the plotted curve and its derivative for each case, as it is summed up in Table 3. As an example, the transference curves derivatives for the L_N/L_P = 1μm/1μm configuration are exhibited in Figure 5.

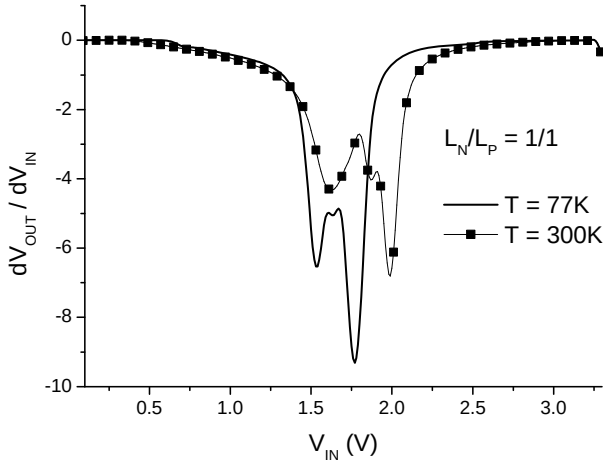

Figure 6 – Voltage gain as a function of the input voltage at 77 and 300 K.

Table 3 – Transition voltage, high noise margin, low noise margin and maximum gain for two different inverters at 77 and 300 K.

	L_N / L_P	300 K	77 K
V_{Tinv} (V)	1 / 1	1.73	1.67
	1 / 3	1.49	1.50
NM_H (V)	1 / 1	1.15	1.35
	1 / 3	1.46	1.57
NM_L (V)	1 / 1	1.28	1.33
	1 / 3	0.89	1.06
Maximum Gain	1 / 1	6.8	9.3
	1 / 3	7.2	10.4

Focusing on the transition voltage, it is clear that it is very stable at different temperatures, mainly with the L_N/L_P = 1/3 configuration, always around the center of the input voltage range.

Analyzing the temperature impact on the noise margins, it is patent that the values increase at 77 K, exactly as it is expectable taking the threshold voltages variation into consideration.

It is also very interesting to highlight the temperature impact on the maximum gain, noticing its patent increase of around 40% at low temperature. This important result may be understood as an extension of the $|V_{th}|$ raises influence on the transference curve maximum slope and the previously explained increase in the noise margins.

Finally, keeping in mind that the Kink Effect influence is evident in the transference curve transition region [7], the increase in the noise margins at 77 K also overshadows the abrupt impact in the standard transference curve format displayed at room temperature.

5. CONCLUSION

In this work, the temperature influence on SOI technology was studied, based on nMOS and pMOS individual transistors and an inverter circuit composed by an association of them.

The I_D x V_{GS} curves revealed an increase of the threshold voltage because of the Fermi potential temperature dependence and an increase of the maximum mobility at very low temperature, resulting in the rise of drain current level in comparison to room temperature values. Particularly in pMOS transistors, a second clearly identifiable threshold voltage may be put down to the emerging Edge Transistor Effect, bringing into sight a parasitic drain current in the main transistor.

Regarding the logic inverter circuit, it was concluded that the transition voltage is quite constant toward the temperature variation. On the other hand, as a consequence of the increase in the nMOS and pMOS $|V_{th}|$, higher values of noise margins were displayed and, accordingly, the maximum gain presented an intense increase of approximately 40%.

From a global point of view, in spite of the undesirable parasitic effect that appeared in SOI pMOS transistors, the inverter exhibited an improved static behavior at 77 K, presenting an undoubtedly better suitability for general technologic purposes.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

[1] Katsutoshi Izumi, Proceedings of the Fourth International Symposium on Silicon-On-Insulator Technology and Devices, Vol. 90-6, p.3, 1990.

[2] W. A. Krull and J. C. Lee, Proceedings of SOS/SOI Technology Workshop, p. 69, 1989.

[3] G. E. Davis et al, IEEE Trans. on Nuclear Science, Vol. 32, p. 4432, 1985.

[4] J. P. Colinge, “Silicon-On-Insulator Technology: Materials to VLSI”, 3rd Edition, Kluwer Academic Publishers, 2004.

[5] J. A. Martino, M. A. Pavanello e P. B. Verdonck, "Caracterização Elétrica de Tecnologia e Dispositivos MOS", Editora Thomson Learning, 2003.

[6] L. Geynet et al, A Fully-Integrated Dual-Band VCO with Power Controlled by Body Voltage in 130 nm CMOS/SOI, in IEEE-NEWCAS Conference, 2005.

[7] M. D. V. Martino, M. Sandri et al, “Radiation Influence on SOI CMOS Devices”, 7th Microelectronics Student Forum