AUTOMATED TEST BENCH FOR OPERATIONAL AMPLIFIERS

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ABSTRACT

This paper introduces a tool for use in Analog IC verification. It does the extraction of operational amplifiers most common characteristics, based on known test benches. The tool combines the use of a SPICE and a Analog HDL simulator (ELDO and ADMS from Mentor Graphics), a calculator (Octave), and a graphic plotter (GnuPlot). It was used to assist the design of basic CMOS operational amplifier, and has saved enough time from simulations. The results for both, reference model and implemented design are presented.

1.INTRODUCTION

In microelectronics, there is a need to improve the circuits efficiency, being time and production cost two factors of big importance. The objective of functional verification is to check all the characteristics of the design and assure that it behaves accordingly to the specifications [1]. The creation of automated testbenches in high level code gives better results in each step of the design, thus minimizing possible mistakes that can occur.

The process of funcional verification can be done during the whole project, being the slowest stage, but it gives techniques capable of reducing the costs of the process, in the idea of economy of time and other factors assisting the project to reach its objectives [2]. This paper reports an automated test bench for helping on the verification of operational amplifier designs.

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2.DESCRIPTION OF THE ATBO

The Automated Test Bench for Opamps (ATBO), it is a set of testbenches used for verification of operational amplifiers that helps, speeding-up the execution verification tasks, thus, contributing to the designer with an automatic and flexible tool. This methodology of verification is based on the comparison between the architecture in study (known as DUV - Design Under Verification) and a Reference Model, which is normally a behavioral model written in a hardware description language for analog and mixed signals such as VHDL-AMS, Verilog-AMS or SystemC-AMS. The verification consists on sending equal stimulus to both blocks, and then observing their respective outputs. The Figure 1 shows a contextual representation of the testbenches.

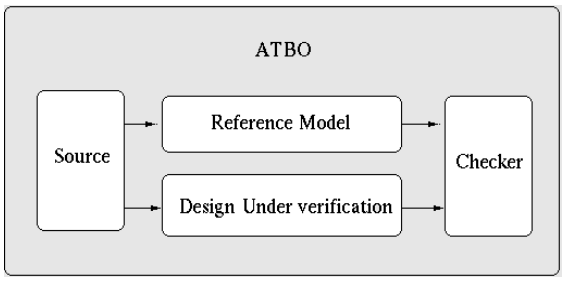

Figure 1: Illustrative diagram of ATBO.

The creation of this flexible tool, based on the methodology of functional verification, requires some essential specifications. The block under verification, must be written in SPICE. The block "Reference Model" is the specified implementation of the system, which is written in one of the following hardware description language: VHDL-AMS, Verilog-AMS or SystemC-AMS [5]. The block "Source" has a very important task in the flow, since it is responsible for generating the input stimulus, and it is made totally in SPICE. The block "Checker" receives the signals from output of the DUV and the reference model, processes the information and

makes a comparison between them, generating the results. This block has a part developed in SPICE, and another one in Octave. The main part of the ATBO, which coordinates the simulations, is a shell script. It is responsible for the interaction of all the programs involved and the user.

The ATBO was developed to be used together with the tools of the Mentor Graphics, that belong to the package IC Nanometer Design, however it can be adapted to use in other compatible tools. ATBO make use of the following programs: SPICE (ELDO) Simulator [3], ADVance MS (ADMS) Simulator, Gnuplot and Octave [6].

3. RESULTS AND DISCUSSIONS

Some results obtained from simulations of the Automated Test Bench for Operational Amplifiers are shown in figures 2,3 and 4. The listen is an output report from the ATBO simulation containing all the extracted information of the simulations. The column Ref shows the results of the Reference Model, the DUV column is from the operational amplifier design. Table 1 shows the description of the figures of merit involved in the verification. As it can be sun, the operational amplifier designed fully complies with the specifications.

Table 1 – Description of the parameters (figures of merit)

Parameter	Description
Ad	Open-Loop Gain [dB]
CMRR	Common Mode Rejection Ratio [dB]
Voffset	Input Voltage Offset [V]
Ioffset	Input Offset Current [A]
Ibias	Input Bias Current [A]
Ricm	Input Common Mode Resistence [Ohms]
Rid	Input Differential Resistence [Ohms]
Icc	Power Supply Current [A]
Iosc	Output Short Circuit Current [A]
PSRR +	Power Supply Rejection Ratio + (VDD) [dB]
PSRR -	Power Supply Rejection Ratio - (VSS) [dB]

The mains parameters of the specification are compared to the simulation results the DUV.

Listing of the parameters (figures of merit) extracted of an operational amplifier (DUV) and a reference model (Ref):

```
#########################################################
    Automated TestBench for Opamps (ATBO)
#########################################################
Parameters                          Ref | DUV
Ad [dB]:                             80 | 98.87
CMRR [dB]:                           80 | 142.2
Bandwidth [MHz]:                  1.585 | 3.162
Phase Margin [degrees]:           90.01 | 62.57
Voffset [mV]:                  0.001005 | 0.008626
Ioffset [mA]:                    0.0002 | 5.5e-15
Ibias [mA]:                      0.0005 | 1.1e-14
Ricm [Ohms]:                      1e+05 | 3.6e+16
Rid [Ohms]:                       1e+06 | 5.4e+20
Icc [mA]:                             3 | 0.01508
Power Consumption [mW]:              60 | 0.3016
Iosc [mA]:                        56.25 | 0.005041
Slew Rate Fall [V/uS]              -0.3 | -1.015
Slew Rate Rise [V/uS]               0.3 | 1.509
Output Voltage Swing (Max V) [V]    4.5 | 2.498
Output Voltage Swing (Min V) [V]   -4.5 | -2.5
PSRR + [dB]                       64.04 | 127
PSRR - [dB]                       64.04 | 129.8
#########################################################
          END OF THE  SIMULATION
    passed time: 01 minute(s) and 04 second(s).
#########################################################
```

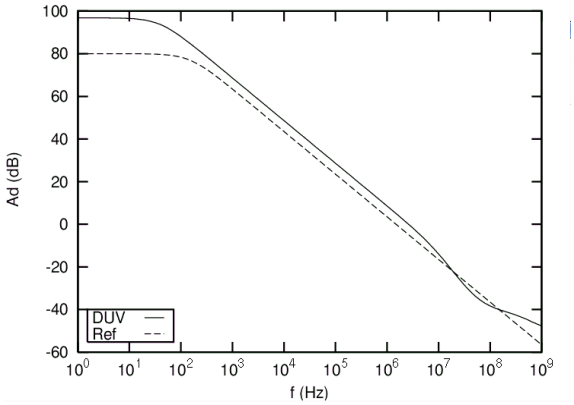

Figure 2: Frequency response of the Open-Loop Gain.

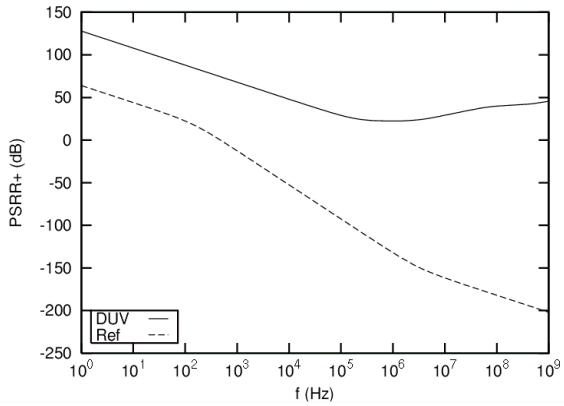

Figure 3: Frequency reponse of PSRR+ (Power Supply Rejection Ratio).

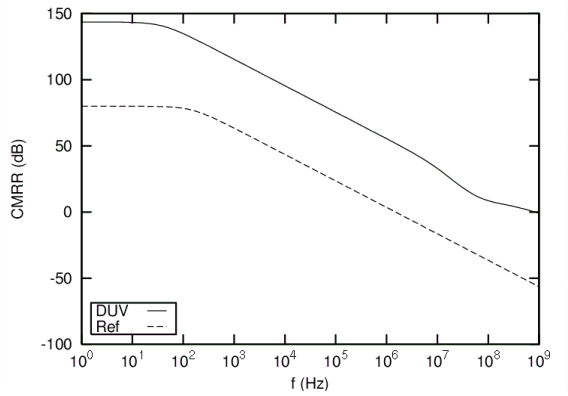

Figure 4: Frequency response of the CMRR (Common Mode Rejection Ratio).

The reference model used in the simulations was written in Verilog-AMS. The operational amplifier (DUV) was designed using devices of AMI 0.5 micron technology, and the simulations results were obtained after pos-layout extraction.

The text above shows the time of efficiency of the generated report purposed for the ATBO.

4.CONCLUSION

The Automated Test Bench for Operational Amplifiers (ATBO) was presented. It helps the designers to fastly verify their designs from outputs written in to files log which shows the performance of the design in comparison to a reference model. The tool lists the most common figures of merit used for validading operational amplifiers, totalizing 18. Simulations extracted have lasted less than 2 minutes to be accomplished. Future works may include the extraction of others figures of merit, and eventually, the extension to other analog blocks.

The main contribution of this work is to offer a tool the accelerates and automatizes the verification of operational amplifiers tasks. Reducing evental by human introduced errors. The results illustrated in the tables and figures show the utility and efficiency of this computational tool created.

5.ACKNOWLEDGEMENTS

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6.ANNEX

6.1 Verilog-AMS model:

```
1  // Operational Amplifier
2  `include "disciplines.vams"
3  `include "constants.vams"
4  module opamp (V1,V2,VDD,VSS,Vo);
5  parameter real G=10000 from [1:inf);
6  parameter real bw=1.5;
7  inout V1, V2, VDD, VSS, Vo;
8  real Ac, Ad, Vout;
9  electrical V1, V2, VDD, VSS, Vout, gnd;
10 ground gnd;
11 analog begin
12 Ac = G/pow(10,CMRR/20);
13 Ad = laplace_nd(V(V1,V2)),{G},{1,G/
   (bw*`M_TWO_PI*1e6)};
14 Vout = Ad + Ac*(V(V1,gnd)+V(V2,gnd))/2;
15 endmodule
```

The above code is a brief resume of the opamp behavioral model. From the twelfth to fourteenth lines, the output receives the common mode and differential mode gain, respectly, with frequency attenuation.

6.2 ATBO main script:

```
1  #!/bin/bash
2  echo "Param. - Ref | DUV" >> results.txt
3  vasim -c -cmd tb1.cir -do do.do
4  octave -q octave1.do
5  gnuplot plota1.plt
6  cat results.txt
```

This code brings the example of commands from the executable file. It is a shell (bash) script coordenating the ATBO actions. The 3rd line calls the ADMS + ELDO simulator, the 4th one extracts the results using the mathematical tool (Octave), and the 5th one plots the simulation graphics with GnuPlot.

6.3 SPICE instances

```
1  * REFERENCE MODEL
2  .MODEL AMPOP MACRO LANG=VERILOG LIB=LIB
3  YAMPOP1 AMPOP PORT: VP1 VN1 VDD1 VSS1 VO1
4
5  * DUV
6  .SUBCKT AMPOPCMOS VP VN VDD VSS VO
     ...
7  .ENDS AMPOPCMOS
8  XAMPOP2 VP2 VN2 VDD2 VSS2 VO2 AMPOPCMOS
```

This code shows how the instantiation of the behavioral model (Verilog-AMS) is made on a SPICE file. Since the testbench and the stimulus are SPICE-compatible, we can add both, the Reference Model and the DUV on this file, and run the simulations using the ADMS + ELDO simulator.

7. REFERENCES

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