ANALYSIS OF MOSFETS ASSOCIATIONS INFLUENCE IN POST-LAYOUT SIMULATIONS

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ABSTRACT

The influence of transistors association techniques in the conception of IC's was analyzed. Pre and post layout circuit's simulations were compared in order to characterize the discrepancies. A current mirror was simulated for miscellaneous equivalents associations and show an error about 60% regarding the expected value for one of the cases. The results show that, in some cases, transistors that should be equivalents present divergent answers.

1. INTRODUCTION

The design flow of any integrated circuit, either digital or analog, has as fundamental step the layout implementation. Although the design tools have reached an automation level never seen before, the layouts construction for analog circuits still is almost entirely made in a manual way.

In the search for the better ratio area/cost, techniques are applied to optimize the space used by the designed circuit. One of the most common is the transistors folding. From series and/or parallel associations, it is possible to reproduce devices with specified W/L through a set of others.

The associations are predicted and described by all models currently know. As show by Montoro *et al*. in [1], series associations lead to the channel length sum, while the parallel ones influence its widht. Transistors association - called Sea of Gates (SOG) or Sea of Transistors (SOT) - are techniques widely employed in designs of IC's and, in addition to enabling the improvement of the ratio area/cost, it can enhance circuit's performance in certain aspects [2], [3].

In this article, we provide comparisons between amplifiers and current mirrors with arbitrary and equivalent specifications, and discuss how the techniques implemented in a layout can influence the results obtained through simulations and its respective relevance for the design of integrated circuits.

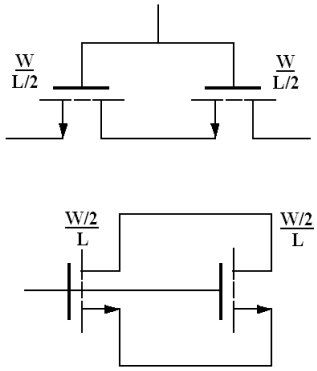

Fig. 1. Series and parallel association of MOSFET's.

2. COMPARATIVE ANALYSES

Despite the equivalence shown by some mathematical models, it is possible to see obvious discrepancies between configurations of equivalent circuits. For instance, some parameters were extracted from an operational amplifier in two cases: in the first (a) the transistors present the W/L aspect concerning to the design; in the second case (b), all transistors were replaced by associations equivalent to the original aspect ratio, representing a post-layout description.

In [2], the authors present a similar case for analyzing the characteristics of two Miller's OTAs with different configurations of association.

Using the SPICE language to describe the circuits and BSIM3v3 models for the AMI 0.5 micron technology with ELDO simulation tool, the results summarized in Table 1 were found:

Parameter	Case a	Case b
Ad (Open Loop)	94.31 dB	91.48 dB
Gain Bandwidth	3.00 MHz	2.63 MHz
Phase margin	63.40 º	67.42 º
CMRR	126.87 dB	131.62 dB
Offset	28.73 µV	40.53 µV
Ios|Ib	0|0	0|0
Ricm|Rid	∞|∞	∞|∞
Icc	20.11 µA	20.05 µA
P. consumption	100.55 µW	100.25 µW
Iosc	3.98 mA	5.01 mA
Output swing +|-	2.5 V|-2.5 V	2.5 V|-2.5 V
PSRR +	98.83 dB	97.69 dB
PSRR -	121.22 dB	118.74 dB
Slew rate fall	0.836 V/µs	0.838 V/µs
Slew rate rise	1.064 V/µs	0.958 V/µs

Tab. 1. Extracted parameters for regular (case a) and associated (case b) op. amps., using BSIM models.

The author is a second year electrical engineering undergraduation student who is engaged in a scientific initiation program sponsored by CNPq.

To understand the real impact of these association techniques, a simpler structure, that is also present in the operational amplifier, was considered.

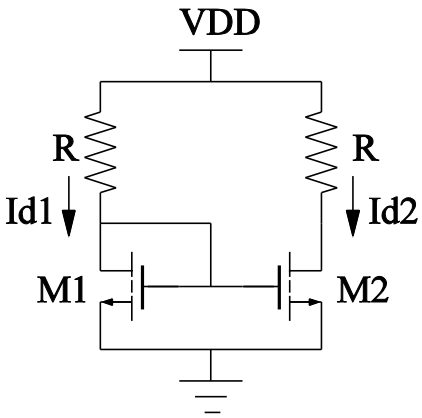

Fig. 2. MOSFET current mirror schematic diagram.

Figure 2 shows a schematic diagram of a current mirror. In this structure, the drain current Id1 of M1 force a common voltage VGS to M1 and M2. Thus, the current Id2 observed in M2 will have value equal to Id1.

For the analysis, various configurations of associations for the transistor M2 were implemented:

- Case 1: 2 transistors in series, each one with W=120µm and L=6µm.
- Case 2: 4 transistors in series, each one with W=120µm and L=3µm.
- Case 3: 8 transistors in series, each one with W=120µm and L=1.5µm.
- Case 4: 2 transistors in parallel, each one with W=60µm and L=12µm.
- Case 5: 4 transistors in parallel, each one with W=30µm and L=12µm.
- Case 6: 8 transistors in parallel, each one with W=15µm and L=12µm.

Using the BSIM3v3 models, level 53, for 0.5 micron technology, using the simulation tool ELDO, the Id2 currents were measured from a DC analysis, ranging from 1,5 V up to VDD and the results are shown in Figures 3 and 4.

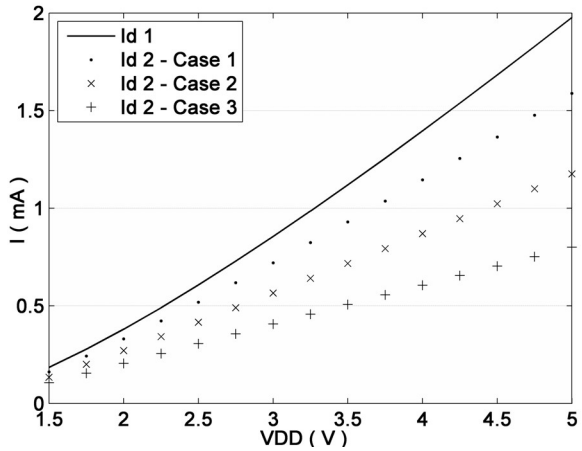

Fig. 3. Id2 current for cases 1, 2 and 3, using BSIM3v3 models.

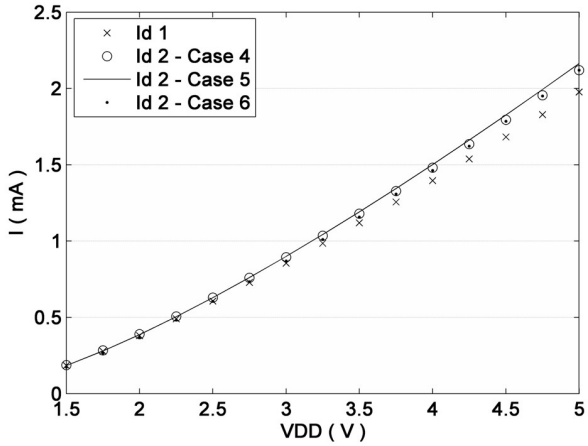

Fig. 4. Id2 current for cases 4, 5 and 6, using BSIM3v3 models.

The simulation shows that the maximum variation between the expected value (Id1) and the measured value (Id2 - case 3) is 60%. It is also possible to see that the discrepancies are more evident in series associations (cases 1, 2 and 3) and are directly proportional to the number of divisions implemented in the transistor. The current measured in the first three cases is always lower than expected. For those cases where the transistors are associated in parallel (cases 4, 5 and 6), the current Id2 presented values above the reference Id1. However, the differences observed were not proportional to the number of divisions and the case 5 presents the highest variation.

Since the transistors M1 and M2 are operating in the saturation region, the current-voltage relationship can be described by the equation [4]

$$Id = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) \quad (1)$$

where λ is related to the channel modulation. In cases 1, 2 and 3, series associations are employed in order to obtain the equivalent transistor M2. Thus, the associated transistors have their channel length reduced and, consequently, the value of λ becomes more representative. In fact, it's expected a change in the current value Id2 for these cases.

Similarly, (1) does not predict any changes for the cases where the transistor was obtained from parallel associations (cases 4, 5 and 6). Since the channel length of each associated transistors is equal to the transistor M2, the modulation channel impact will be the same and the current value Id2 should be equal in these situations..

However, the simulated results show a variation far beyond the predicted by mathematical models.

Fiorelli *et all.* showed in [5] the use of series-parallel associations in current mirrors. Besides obtaining the expected value to current mirror, the authors presented advantages in the use of SOT.

The equivalence reached through the transistors associations is proved mathematically. In [6] the authors conducted detailed comparisons between EKV and BSIM3v3 models and concluded that although the

transconductance has been properly modeled in both models for strong and weak inversion, the BSIM3v3 presented an error of approximately 40% for the moderate inversion, while the EKV proved to be close to ideal.

In the search for more consistent results, the same current mirror - and their associated settings - was simulated in SPICE in the same conditions, but using the EKV2.6 models, level 44, instead of BSIM3v3 for 0.5 micron technology. The results are shown in Figures 5 and 6.

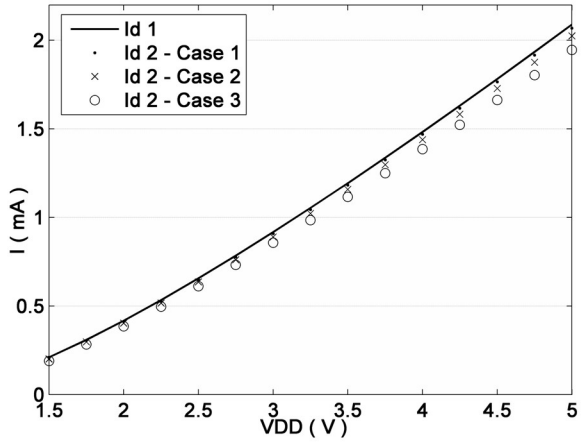

Fig. 5. Id2 current for cases 1, 2 and 3, using EKV models.

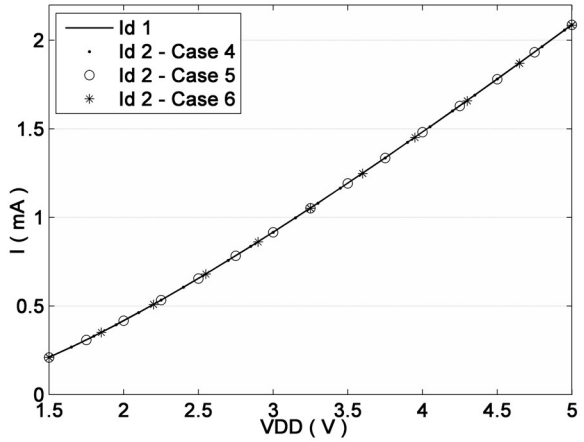

Fig. 6. Id2 current for cases 4, 5 and 6, using EKV models.

The results show that the maximum variation between the expected value of current Id2 and the measured is only 9.5%. For cases 4, 5 and 6, when the transistors are connected in parallel, the variation is almost zero.

In the analysis of the operational amplifier, the EKV models also showed more subtle discrepancies. For instance, using the BSIM3v3 was observed a variation between the two equivalent settings of about 12.5% for the gain bandwidth and 20.5% for the output short circuit current. Using the EKV models, the variation observed was about 1% for both parameters. The complete set of extracted parameters using EKV model can be seen in Table 2.

Parameter	Case a	Case b
Ad (Open Loop)	97.39 dB	97.52 dB
Gain Bandwidth	2.42 MHz	2.45 MHz
Phase margin	52.75 º	57.17 º
CMRR	149.79 dB	143.95 dB
Offset	4.10 µV	3.91 µV
Ios|Ib	0|0	0|0
Ricm|Rid	∞|∞	∞|∞
Icc	20.12 µA	20.12 µA
P. consumption	100.60 µW	100.60 µW
Iosc	4.97 mA	5.01 mA
Output swing +|-	2.5 V|-2.5 V	2.5 V|-2.5 V
PSRR +	97.04 dB	97.20 dB
PSRR -	164.38 dB	164.61 dB
Slew rate fall	0.824 V/µs	0.814 V/µs
Slew rate rise	0.902 V/µs	0.932 V/µs

Tab. 2. Extracted parameters for regular (case a) and associated (case b) op. amps., using EKV models

The BSIM [7] and EKV models [8] are based on different principles. Moreover, the BSIM was first developed in order to meet general purposes, while EKV was developed specifically to meet the needs of low-voltage and low-current analog circuits designers. Often the models are compared under specific conditions in order to determine which one better provides the circuits answers [9].

The comparisons made in this paper does not determine which model best describes the circuit's behavior, only shows how each one responds to the associations used in transistors.

3. CONCLUSION

This article presented simulated results for typical and post-layout circuits descriptions. It presented a comparison of amplifiers with and without association techniques. Similar analyses were performed in a common current mirror. A comparison between BSIM and EKV models was also held in order to determine how the models interpret the equivalent associations that are often used in the final descriptions of circuits – layouts. In this aspect, the EKV model presents answers more consistent to the expected values.

The physical implementation, along with post-layout simulation, are critical steps in the designing process of integrated circuits. However, simulations based on a consolidated model as the BSIM, show that the characteristics of associated transistors are not reproduced on a completely faithful way.

The development of design tools contributes to increase the number of IC's designs that become real. In addition to facilitating the process, such tools have evolved in order to deliver simulated results even closer to reality. However, it is necessary to analyze and interpret the results before employ changes to the physical description of the circuit - layout - with the goal of achieving better responses to simulated stimuli.

The mathematical models that describe the characteristics of devices and are used in designs simulations, have a high level of complexity. Still, they

have strengths and weaknesses. The prior knowledge of these characteristics may determine the creation of a good design and avoid surprises after prototyping.

4. ACKNOWLEDGEMENTS

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5. REFERENCES

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