

# AN INTERFACE FOR NOC-BASED VIRTUAL PLATFORMS SIMULATION

Camila N. de Oliveira<sup>[1,2]</sup>, Silvio Fernandes<sup>[1,2]</sup>, Bruno C. Oliveira<sup>[1,2]</sup>, Ivan S. Saraiva<sup>[1]</sup>

[1] Departamento de Informática e Matemática Aplicada,  
Universidade Federal do Rio Grande do Norte, Natal, Brasil  
camila@lasic.ufrn.br, silvio@lasic.ufrn.br, bcruz@lasic.ufrn.br, ivan@dimap.ufrn.br

## ABSTRACT

Nowadays, there are a lot of research and development being made with virtual platforms, due to their complexity and diversity of configurable parameters. The parameters' configuration is exhaustive and is often responsible for errors, especially because of the great amount of simulations necessary. Regarding this problem, we developed an interface to make the designers' lives easier and avoid the number of mistakes made by them. This interface was developed to comply with platforms that have NoC as an interconnection mechanism. Research shows that interfaces are more suitable than command lines to avoid errors. The developed interface aims to present a good visual aspect, to be intuitive to the user and easy to handle. This is achieved by automating most part of the tasks, in order to reduce the number of mistakes made by the designer.

## 1. INTRODUCTION

The manufacturing in the hardware industry is driven by the concept of time-to-market [1]. In this sense, the design process must be as reliable and fast as possible, and the mechanisms to ensure this pose as a great challenge to the academic researchers, whose new scientific contributions attend the pressing urge of the industry.

The design tools have been indispensable for any project, and can be applied in the elaboration, design, prototyping, synthesis or test stages. Generally, these tools are related to or use hardware description languages, such as VHDL and Verilog.

On the other hand, there are several researches that are developed using the SystemC language [2], which allows to design and simulate in different levels of abstraction. Thus, it is possible to evaluate a project from the functional level to the cycle-accurate level. However, the hardware designer has also to implement the simulator to do experiments with the hardware project.

The group of integrated systems development from LASIC (*Laboratório de Sistemas Integrados em Chip*) have done research related to reconfiguration [3], network-on-chip [4], applications [5], [6], [7] and virtual platforms [8], [9]. Some of these researches are

developed in SystemC, in particular the virtual platforms<sup>2</sup> STORM [8] and IPNoSys [9]. Both of them are implemented in SystemC using a high (though cycle-accurate) level of modeling abstraction called Transaction Level Modeling (TLM).

In the simulations of both platforms, many configuration parameters are used to allow the instance of different versions of them. This paper proposes a software interface which allows configuring and simulating NoC-based platforms, such as STORM and IPNoSys.

This paper is organized as follows: the second and third sections present a brief explanation about the IPNoSys and STORM, respectively. In the fourth section the interface proposed is presented and the last section contain the conclusions and future works.

## 2. IPNOSYS

The more traditional direct NoC design consists on a set of routers interconnected with a computing element, a memory or other useful core in a computing system. The IPNoSys (Integrated Processing NoC System) is a novel NoC-based parallel architecture in which the NoC is not only an interconnection mechanism, but also is responsible for the execution of applications. In this architecture the routers are able to perform the application's instructions, further on routing the packets that flow through the NoC channels. So, the IPNoSys architecture does not use Von Neumann processors, thus, the routers become Routing and Processing Unit (RPU) and in the network's corners there are Memory Access Cores (MACs), where the four memory modules are placed.

The applications are described in the IPNoSys packet format that includes the operations and its operands. An application could be described through one or more packets depending on the data dependencies and parallelism strategy. These packets are stored in the memory modules and injected by the MACs.

The IPNoSys uses an own routing algorithm, called spiral complement, since it combines the XY routing police and the complement traffic pattern. This routing

---

<sup>2</sup> This work was supported in part by the "Agência Nacional do Petróleo (ANP)".

algorithm guarantees that all operations into the packet are performed independent on the amount of operations and the NoC dimensions. This algorithm allows finding a new destination to a packet when it arrives at its destination and its operations remain to be performed. This architecture with the algorithm also identifies and avoids deadlock situations.

The simulations and evaluations show that IPNoSys is a fully scalable architecture which has a great potential to parallel processing and the chip area, and possibly power dissipation, can be substantially reduced due the processors absence.

### 3. STORM

STORM is a customizable Multi-Processor System-on-Chip (MPSoC). The platform is designed to support up to 256 cores. Its objectives are: to produce a real and fully functional MPSoC platform that actually runs binary compiled codes of complete applications written in a high level language (C language), and to be able to provide a set of results especially useful in design-space exploration. These results regard microprocessor execution, NoC communication and memory hierarchy overhead.

Since it is a platform, STORM does not present a fixed architecture. Its supported cores can be placed anywhere in the NoC and its architecture is identified during the boot process. Currently, this platform supports the integration of SPARC V8 processor with cache modules (data cache and instruction cache); and a memory module which is associated to a directory module. Any other SystemC module can be placed in the platform as long as it follows its standard NoC communication protocol.

Currently, this platform can integrate the SPARC V8 processor with two kinds of memory models: shared or distributed. In the shared memory model, the designer can configure the cache, as the cache coherency mechanism is directory-based. The platform also has a mechanism to access the memory in atomic way.

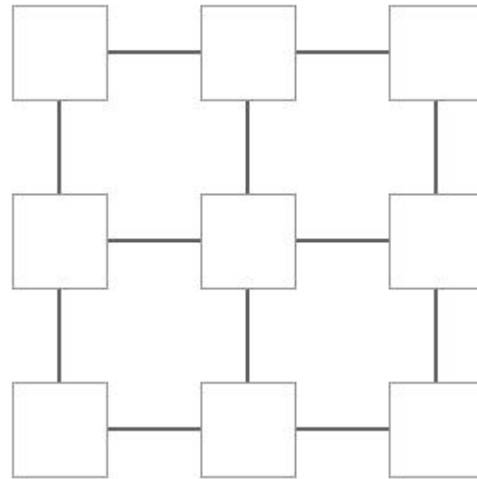
The STORM allows the designer to simulate many MP-SoC architecture versions, providing a powerful tool for exploration of design space. The capacity of expansion combined with several configurable parameters allows the study of the MP-SoC environment aspects.

### 4. THE INTERFACE

As for the most of hardware projects in SystemC, it was developed software simulators for the STORM and IPNoSys platforms which allow simulating their behavior while they execute applications, further obtaining the results to evaluate the platforms' performance.

In general, the SystemC simulators are developed with lots of parameters that can be configured, that allow simulating different versions of the hardware architecture. The parameters can be set through command line, as argument, while the simulator is being called or

they can be written in a file that is read by the simulator to start the simulation. STORM and IPNoSys use the second strategy.



**Figure 1 – Mesh topology**

However, in both of the configuration strategies, mainly the first one, there is a risk to make mistakes. Furthermore, the designer is responsible to control the combination of all the parameters to achieve different scenarios for the simulations, what turns the simulation task very meticulous.

In this sense, it is proposed a software interface to configure and simulate NoC-based platforms. This interface was implemented in Qt 4 [10], a cross-platform application framework for desktop with a rich C++ class library for GUI development. Qt 4 has a GPL (General Public License) license, is portable and the STORM and IPNoSys platforms are also implemented in SystemC/C++.

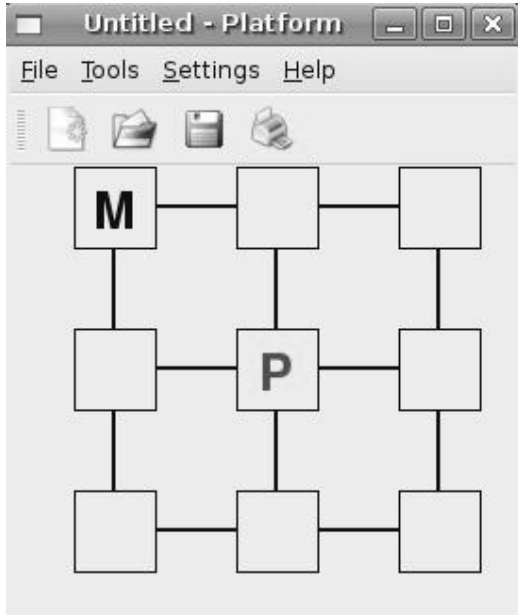
Therefore, this interface aims to support the configuration, simulation and results reporting processes in NoC-based platforms. The interface allows accelerating these processes and avoiding mistakes, once the configuration is fulfilled through dialog boxes which verify or restrict the values' field in its range. Furthermore, the interface can organize the combination of the parameters, saving profiles that can be used in lot of simulations in the same platform or in similar simulations in different platforms in order to compare them. The interface also is a tool to standardize the input parameters and simulations results.

Currently, this interface can be used in 2D-mesh NoC (Figure 1), as STORM and IPNoSys, but will be extend to other topologies. The main three interface's functionalities are: configuration, simulation and results report, which are presented following.

#### 4.1. Configuration

The interface provides methods to configure specific and general parameters of a platform. The general parameters are related with the topology and amount of nodes

(routers and/or cores). The specific parameters are: core type, memory size and location.



**Figure 2 – Platform Preview**

Currently, the interface allows configuring only the STORM and IPNoSys platforms. Meanwhile, only the mesh topology is supported.

Through the menu it is possible to choose which of the two platforms are used and set the specific parameters. Before that, the general parameters must be set, and then the interface shows a preview of the platform, with the nodes and its links, as presented in Figure 2. Clicking in a node in the preview displays a pop-up menu to configure the node. This way avoids mistakes and allows the increase of future functionalities.

In the configuration process it is also possible to define the memory organization for an interaction with the compiler that will generate the code which will be executed in the platform. This function is useful to configure linker scripts that inform to the linker which parts of the code contain the variables that must be allocated. The interface generates these scripts through the information provided by the designer.

The configuration can be saved in file and it is possible to use it for many simulations.

#### 4.2. Simulation

After the configuration, the platform is ready to simulation. In general, the simulations in complex platforms take long time, thus, to decrease the time necessary to simulate, it is common to do a distributed simulation, using more than one computer. The interface allows the designer to configure and execute the simulation in distributed environments.

Other task realized by the interface is the generation of execution packets. An execution packet contains a whole configuration of a platform and the code of the

application necessary to simulate it. This mechanism allows remote simulations without any access restriction.

#### 4.3. Reporting results

The evaluation of architecture's performance in SystemC is done through results obtained by the simulator. Many results can be obtained; however, the computing and the report of them are implemented by the simulator programmer. Thus, each architecture can implement and report its own results.

Therefore, the interface aims at the standardization of the results report. The communication among the interface and the other architecture's modules is realized through the standard methods that report the results, as an API. Thus, through them it is generated the report of the results, such as execution time, required memory and average bandwidth.

### 5. CONCLUSION

It was presented a software interface for NoC-based platforms simulation in SystemC. Such interface aims to be a generic tool for design of NoC-based platforms. Currently this interface supports the STORM and IPNoSys platforms, both with the mesh topology.

The interface is a tool that is linked to the virtual platforms to speed up the configuration, simulation and result report processes and avoid mistakes. It is possible to configure, visualize and save the configuration of a platform, do simulations locally or remotely and report results in a standard way.

The use of the interface with the STORM and IPNoSys platforms was successful in the three processes. Thus, it was possible to speed up the validation and performance evaluation through the results analysis.

Future works include mechanisms to support other platforms, with other topologies and including specific characteristics. The interface can automatically combine all the parameters and the designer choice of which it will be simulated. Alternatively, it also can simulate these combinations and report the results.

### 6. REFERENCES

- [1] S. Madeira, "Um Ambiente Baseado em Componentes para Desenvolvimento de Softwares de Sistemas Embutidos." vol. Mestrado Santa Catarina: Universidade Federal de Santa Catarina, 2004.
- [2] OSCI, "SystemC," 2005.
- [3] M. M. Pereira, B. C. d. Oliveira, and I. S. Silva, "RoSA: a reconfigurable stream-based architecture," in *Proceedings of the 20th annual conference on Integrated circuits and systems design* Copacabana, Rio de Janeiro: ACM, 2007.
- [4] R. Soares, I. S. Silva, and A. Azevedo, "When reconfigurable architecture meets network-on-chip," in

*Proceedings of the 17th symposium on Integrated circuits and system design* Pernambuco, Brazil: ACM, 2004.

[5] G. Girão, S. R. F. Araújo, M. M. Pereira, and I. S. Silva, "Implementation of a HDTV transport stream multiplexer based on ITU-T H.222.0 recommendation," in *Proceedings of the 11th Brazilian Symposium on Multimedia and the web* Pocos de Caldas - Minas Gerais, Brazil: ACM, 2005.

[6] M. Carvalho, S. R. F. Araújo, G. Girão, and M. M. Pereira, "Estimação de Movimento em Hardware para o Projeto SBTVD Utilizando o Algoritmo de Busca Completa," in *IV Workshop Técnico Científico do DIMAp – 20 Anos – Artigos Selecionados*. vol. 1, A. M. Moreira and U. S. d. Costa., Eds. Natal: EDUFRN, 2006, pp. 36-47.

[7] M. M. Pereira, S. R. F. d. Araújo, B. Oliveira, and I. S. Silva, "Using traditional loop unrolling to fit application on a new hybrid reconfigurable architecture," in *23rd Annual ACM Symposium on Applied Computing*, Fortaleza, 2008.

[8] R. S. d. L. S. Rego, "Projeto e Implementação de uma Plataforma MP-SoC usando SystemC," in *Departamento de Informática e Matemática Aplicada*. vol. Mestrado Natal: Universidade Federal do Rio Grande do Norte, 2006, p. 144.

[9] Araújo, S. R. F. de. *Estudo da Viabilidade do Desenvolvimento de Sistemas Integrados Baseados em Redes em Chips sem Processadores: Sistema IPNoSys* in Departamento de Informática e Matemática Aplicada. vol. Mestrado Natal: Universidade Federal do Rio Grande do Norte, 2008, p 74.

[10] Qt Reference Documentation (Open Source Edition). Available at: <http://doc.trolltech.com/4.0/index.html>.