AUTOMATIC SYNTHESIS OF ANALOG BASIC BLOCKS USING A SIMULATED-BASED ALGORITHM AND COMPACT MOSFET MODEL

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ABSTRACT

This paper proposes a methodology for automatic synthesis of analog basic building blocks. The methodology is based on the minimization of a cost function composed by the variables of an analog block (transistor lengths and widths). The implementation was made in Matlab, with a generic non-linear optimization function and an external electrical simulator for the evaluation of circuit specifications. The MOSFET model used was ACM, which has a reduced set of technology parameters and is continuous in all regions of operation. As example, we present the design of a differential amplifier.

1. INTRODUCTION

Automatic synthesis of analog integrated circuits can be very useful in microelectronics design, because it provides an efficient search for the circuit variables, among a set of design characteristics, to make it more efficient as possible. Several works have been done in this area, aiming the development of tools for the automation of time-consuming tasks and complex searches in highly non-linear design spaces [1, 2, 3]. However, as far as we know, there is not a commercial tool capable to perform the synthesis of analog circuits with optimum results in a feasible time. An important improvement in the analog design could be the automation of some design stages, such as transistor sizing and layout generation [4], maintaining the interaction with the human designer. The large number of design variables and the consequent large design space turn this task extremely difficult to perform even for most advanced computational systems. In this context, we propose an automatic synthesis procedure for basic analog building blocks which can generate sized transistors with efficient time and computational resources. The synthesis procedure has as main strategy the local search using a generic optimization algorithm and the interaction with an electric simulator. The circuit generated is simulated and the performance results are compared with the last results obtained in order to verify the quality of the new solution.

This work is organized as follow: section 2 shows the description of the proposed methodology; section 3 presents the application of the methodology in the design of a specific analog block - the differential amplifier - with circuit description and final results; finally, in section 4 are shown the conclusions.

2. DESCRIPTION OF THE METHODOLOGY

The methodology used is based on the minimization of a cost function. The cost function, used in this synthesis, is a sum of area and power consumption. The minimization of the function depends on the input specifications and must be inside a limited region given by a restriction function. The values to calculate the cost function and restriction function are obtained through the results of electrical simulations of the circuit. The synthesis procedure was implemented in Matlab [5] in order to minimize a cost function defined as the sum of the total silicon area and the power dissipation in a basic analog block. These two functions are calculated by DC electrical simulations using Smash simulator [6] and ACM MOSFET model [7]. Fig. 1 shows the proposed design flow. The algorithm was implemented in Matlab using the minimization function for non-linear systems *fmincon*, which finds a constrained minimum of a function of several variables [8]. It receives as input the initial value of variables of the analog block. Based on this input, it runs an external electrical simulator, reads the simulator output and calculates the performance functions. After, it modifies the variables (performing a small perturbation) and repeats the procedure until a result that meets the desired specifications.

The function *fmincon* is specific for local optimization, resulting in a small perturbation in the variables inside the design space, respecting design constraints. As consequence, the convergence of *fmincon* is highly related to the variables initial values, which can be estimated with a first-order manual design using simplified design equations.

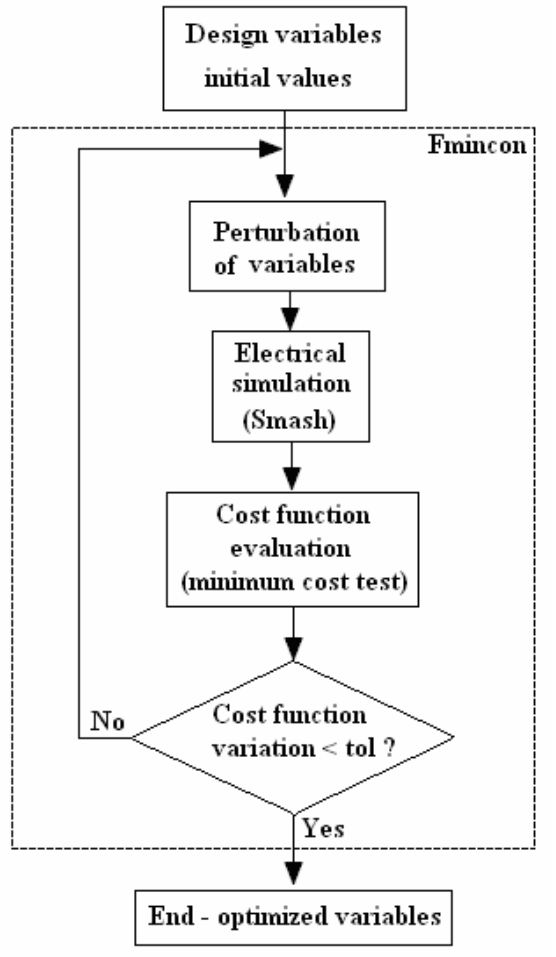


Fig. 1 – Proposed design flow

3. DESIGN EXAMPLE: DIFFERENTIAL AMPLIFIER

The differential amplifier is one of the most versatile circuits in analog design. It is compatible with ordinary CMOS integrated-circuit technology and serves as the input stage to op amps [9]. Its basic function is to amplify the difference voltage between the inputs. The circuit is basically formed by a load current mirror (M3 and M4), a source-coupled differential pair (M1 and M2) and a reference current mirror (M5 and M6), shown in Fig. 2. The main parameters of the circuit are: low-frequency voltage gain (Av_0), gain-bandwidth product (GBW), slew-rate (SR), input common-mode range (ICMR), dissipated power (Pdiss), area (A), etc.

The low-frequency gain is the relationship between output and input, defined as:

$$Av_0 = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \quad \text{(eq. 1)}$$

where g_{m1} is the gate transconductance of transistor M1 and g_{ds2} and g_{ds4} are the output conductance of M2 and M4, respectively.

The slew rate (SR) is the maximum output-voltage rate, either positive or negative, given by:

$$SR = \frac{I_{ref}}{C_1} \quad \text{(eq. 2)}$$

where, I_{ref} is the current in transistor M5 and C_1 is the total output capacitance. This capacitance is estimated as the sum of the load capacitance CL and drain capacitance of M2 and M4. Input common-mode rate (ICMR) is the maximum or minimum input common-mode voltage, defined as:

$$ICMR^- = v_{DS5(sat)} + v_{GS1} + v_{SS} \quad \text{(eq. 3)}$$

$$ICMR^+ = v_{DD} + v_{GS3} + v_{TN1} \quad \text{(eq. 4)}$$

Here, $v_{DS5(sat)}$ is the saturation voltage of transistor M5, v_{GS1} and v_{GS3} are gate-source voltage of M1 and M3, respectively, v_{DD} and v_{SS} are voltage sources of circuit and v_{TN1} is the threshold voltage of M_1. The gain-bandwidth product given by:

$$GBW = \frac{g_{m1}}{C_1} \quad \text{(eq. 5)}$$

Based on the equations above, the initial values for the circuit were estimated, shown in Tab. 1, where W and L are width and length of transistors, respectively. The size of transistors M3 and M4, M1 and M2, and M5 and M6 are equal due to the requirement of matching in the load current mirror, source-coupled differential pair and reference current mirror.

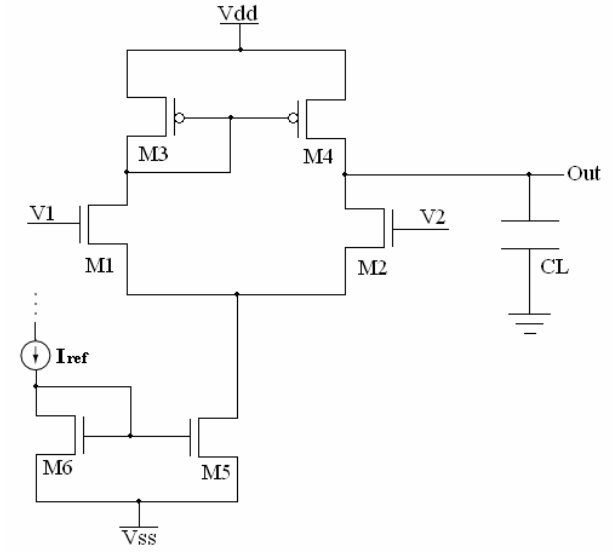


Fig. 2: Schematics of a differential amplifier

Tab. 1 – Design variables for the differential amplifier

Variable	Designed Value
$W_{(M1, M2)}$	20µm
$W_{(M3, M4)}$	30µm
$W_{(M5, M6)}$	100µm
$L_{(M1, M2)}$	10µm
$L_{(M3, M4)}$	15µm
$L_{(M5, M6)}$	5µm
Iref	50µA

The cost function used in this work for the differential amplifier considers a trade-off between area and power consumption, given by:

$$fc = \frac{2.(W_{M1}.L_{M1} + W_{M3}.L_{M3} + W_{M5}.L_{M5})}{A_0} + \frac{I_{ref}.(v_{dd} + |v_{ss}|)}{P_0} \quad \text{(eq. 6)}$$

where A_0 and P_0 are the area and power consumption of reference, evaluated with initial values.

3.1 Synthesis Results

In order to evaluate the proposed automatic synthesis methodology, we performed a design example. The specifications and restrictions used are shown in Tab. 2.
The algorithm was executed in a personal computer with Pentium D 3.0GHz processor and 512MB of RAM. The optimization procedure was performed in 6 minutes for 100 iterations, which is can be considered acceptable for this purpose. In Fig. 3 is shown the evolution of objective function (cost function). In this figure it is possible to note that several variations occurred in the value of the function until it stabilize. Also, it is important to inform that the minimum value is not the optimum point, because the smaller value of cost function does not satisfy the initial specifications (restriction function), and thus it does not serve as final value. In Fig. 4 is shown the variation of some variables of the circuit. It is possible to see that the values of the variables are reduced along the iterations until reaching an optimized value. The final circuit specification and transistor sizes are shown in Tab. 3 and Tab. 4, respectively.

Tab. 2 – Design specifications

Parameter	*Value*
Av_0	60dB
SR	5 V/µs
$ICMR^+$	0.7V
$ICMR^-$	-0.7V
GBW	4.5MHz

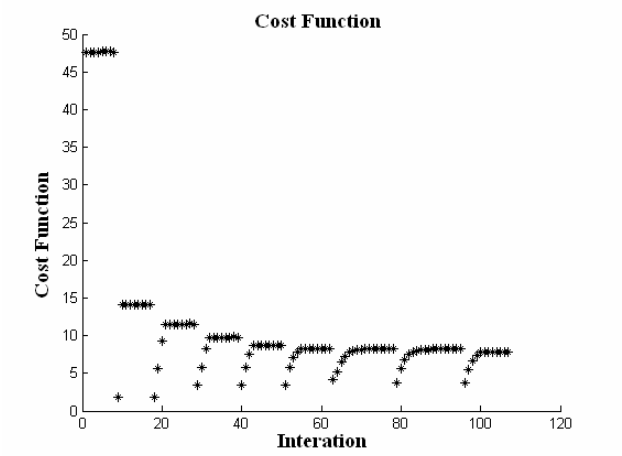
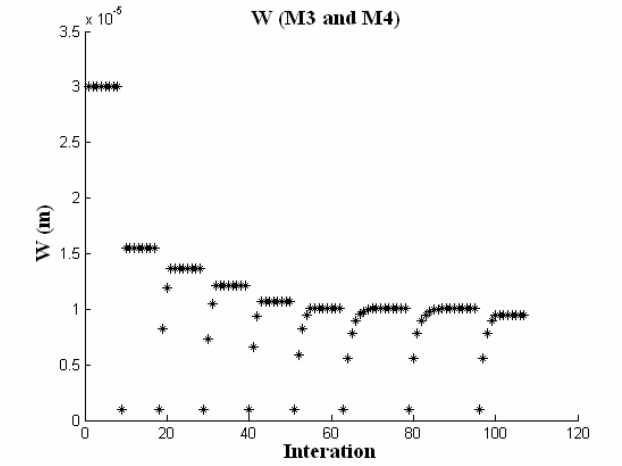
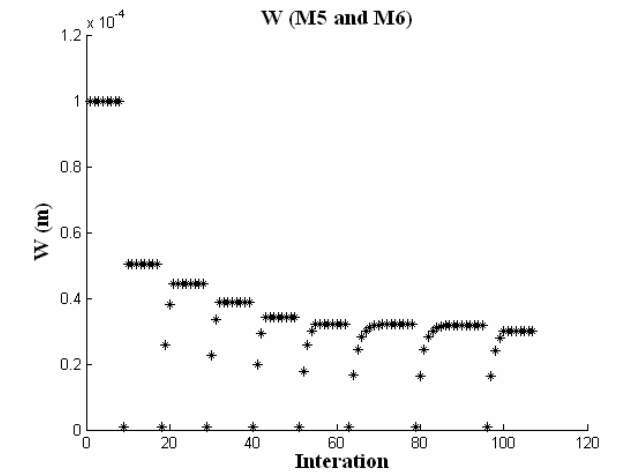


Fig. 3: Cost function evolution



(a)



(b)

Fig. 4: Evolution of design variables. a) $W_{(M3,M4)}$; b) $L_{(M5, M6)}$

Tab. 3: Final values of variables for the differential amplifier

Variable	Designed Value
$W_{(M1, M2)}$	9.00 µm
$W_{(M3, M4)}$	9.49 µm
$W_{(M5, M6)}$	30.00 µm
$L_{(M1, M2)}$	4.98 µm
$L_{(M3, M4)}$	5.93 µm
$L_{(M5, M6)}$	1.71µm
Iref	50.01µA

Tab. 4: Final specifications

Parameter	*Value*
Gain	60.00 dB
SR	5.09 V/µs
ICMR $^{+}$	0.89 V
ICMR $^{-}$	-0.85 V
GBW	4.59 MHz

After the implementation of the algorithm, the results – transistor sizes - were simulated in Smash simulator for checking if it meets specifications (constraints). In Fig. 5 is shown the simulated Bode diagram.

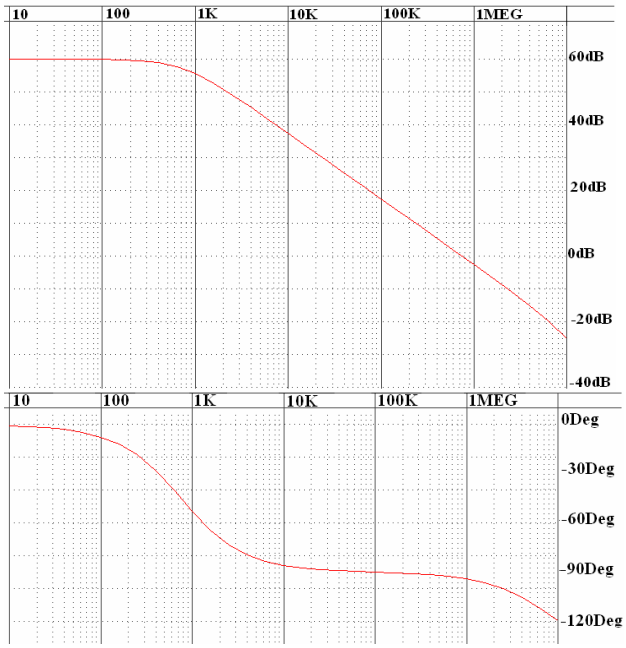


Fig 5: Bode diagram

4. CONCLUSION AND FUTURE WORK

The proposed methodology for automatic synthesis of analog basic building blocks showed good results, in a reasonable time, considering the specifications of area and power. The integration of an optimization algorithm with the electrical simulator guarantees the feasibility of the final solution. As future work, we intend to analyze other cost functions and optimization algorithms, to expand the methodology to other analog blocks and to create an interface with human designer.

5. ACKNOWLEDGMENTS

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6. REFERENCES

[1] M. Degrauwe, O. Nys, E. Dukstra, J. Rijmenants, S. Bitz, B. L. A. G. Go®art, E. A. Vittoz, S.Cserveny, C. Meixenberger, G. V. der Stappen, and H. J. Oguey, IDAC: An interactive design tool for analog CMOS Circuits, IEEE Journal of Solid-State Circuits, SC-22(6):1106{1116, December 1987

[2] M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, Optimal design of a CMOS op-amp via geometric Programming, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, 20(1):1{21, January 2001.

[3]A. Girardi and S. Bampi, Power Constrained Design Optimization of analog Circuits Based on Physical gm/ID characteristics, SBCCI, September 2006.

[4] A. Girardi and S. Bampi, LIT - An Automatic Layout Generation Tool for Trapezoidal Association of Transistors for Basic Analog Building Blocks, Design automation and teste in Europe, 2003.

[5] Stephen J. Chapman, Matlab programming for engineers, Thonsom, Australia, 2003.

[6] AMS simulation, Smash simulator, documentation Dolphin integration, available in <http:// www.dolphin.fr/medal/smash/smash_overview.php>.

[7] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, An MOS transistor model for analog circuit design. IEEE Journal of Solid-State Circuits, 33(10):1510{1519, October 1998.

[8] MathWorks, Matlab - Optimization Toolbox, documentation of MathWorks, available in <http://www.mathworks.com/access/helpdesk/help/toolbox/optim/>.

[9] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, Oxford University Press, Oxford, second Edition, 2002.