3D-NUMERICAL SIMULATION OF THE SOI-FINFET

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ABSTRACT

This paper presents the results of a 3D-numerical simulation of the SOI-FinFET geometry and process parameters for analog circuit design. A 3D-device structure, based on technology standards, is described and simulated. I_D-V_G characteristics are presented and the threshold voltage (V_T) and sub-threshold slope (S) dependence with silicon fin thickness (T_{fin}) and doping (N_A) are shown. The influence of a partial depleted (PD) or fully depleted (FD) silicon fin on device characteristics is also put in evidence.

1. INTRODUCTION

Silicon-on-Insulator (SOI) technology, with single-gate (SG) SOI-MOSFETs, has become in the last years a serious competitor for traditional BULK technology. Double-gate (DG) SOI-MOSFETs have superior performance over single-gate ones. SOI-FinFETs, also called DG-SOI MOSFETs [1] have demonstrated a good potential for circuit applications, in particular low-voltage analog applications [2-5]. Geometry and process parameters optimization are a key factor to increase the performance of the SOI-FinFET for circuit design and fabrication. 3-D numerical simulation is a powerful tool to model and study the device characteristics and it has been extensive used [2-5]. This work presents the results of a 3D-numerical simulation study of the FinFET geometry and process parameters for analog circuit design. Short-channel effects are not investigated in this work and only long-channel devices are addressed.

2. FINFET STRUCTURE AND SIMULATION

A double-gate n-type SOI-FinFET structure, based on technology standards, was described, including the intrinsic part of the fin controlled by the gate, the source and drain fin extensions and pads. The source and drain pads were omitted in the simulations for the sake of simplicity and reasonable computational times. This structure is shown in Fig.1 with the critical dimensions indicated. The doping concentration of silicon fin (N_A) varies from $6x10^{17}$ to $6x10^{18}$ #/cm^3 and the source and drain are doped with a lateral profile with a peak of $1x10^{19}$ #/cm^3. Buried oxide (BOX) thickness (T_{Box}) and the silicon fin height (H_{fin}) are 150nm and 60nm, respectively. Silicon fin thickness (T_{fin}) varies from 20nm to 200nm and the lateral-gate oxide (t_{ox}) is 2nm. The top-gate oxide is ten times (10x) thicker than the lateral-gate oxide to avoid the influence of the first on device characteristics. This top-gate oxide acts like a "hard mask" and avoids the formation of parasitic inversion regions at the top of the silicon fin. The physical gate length (L_G) is 1μm (long-channel FinFET) and the contacts are defined as neutral to avoid a definition of gate electrode work-function. The basic DC electrical characteristics of the SOI-FinFET structure described in the last section were simulated using Davinci [6].

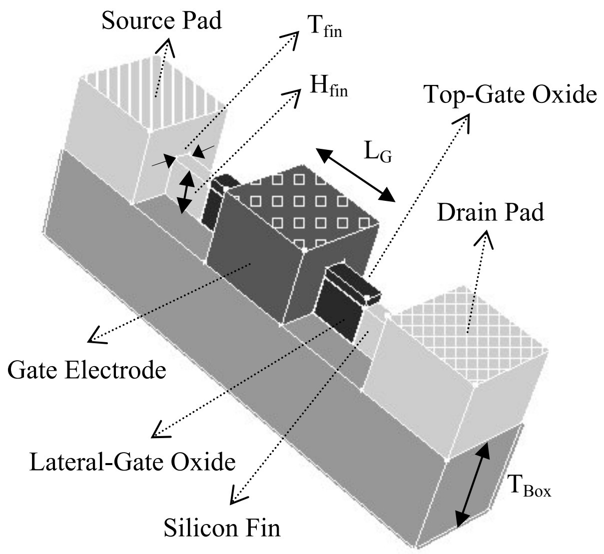

Fig.1 – Basic 3-D SOI-FinFET structure. The critical dimensions are indicated.

3. RESULTS

The simulated I_D-V_G characteristics are shown in Fig.2 and 6 (linear scale) and Fig.3 and 7 (log scale) for different silicon fin thickness (T_{fin}), doping (N_A) and gate oxide thickness (t_{ox}). The currents are normalized by the effective FinFET (double-gate) channel width (W_{eff} = $2xH_{fin}$) to facilitate the comparison with single-gate MOSFETs. The threshold voltages (V_T) were extracted using the maximum transconductance (g_m) method. The results are summarized in the Tab.1.

The values of V_T and S were extracted from Fig.2 and 3 and are shown in Fig.4 and 5, respectively, as a function of T_{fin}. The V_T increases as T_{Fin} increases and tends to saturate in the transition from FD to PD fins. The transition occurs around T_{fin} of 100nm (see Fig.2 and 4). As T_{fin} decreases the total depletion charge (Q_D) contribution to V_T decreases and becomes small compared to the contribution of the gate electrode to silicon work-function difference (ϕ_{ms}) and tends to be negligible. Also for fins thin enough a quantum effect of electron quantization energy has to be considered [1]. These quantum-mechanical effects are not subject of this work. The gate dielectric charge (Q_{ox}=1x10^{12} #/cm^2) contribution to V_T can be considered small. The sub-threshold slope (S) is greatly affected in the transition from FD to PD fins (see Fig.3 and 5).

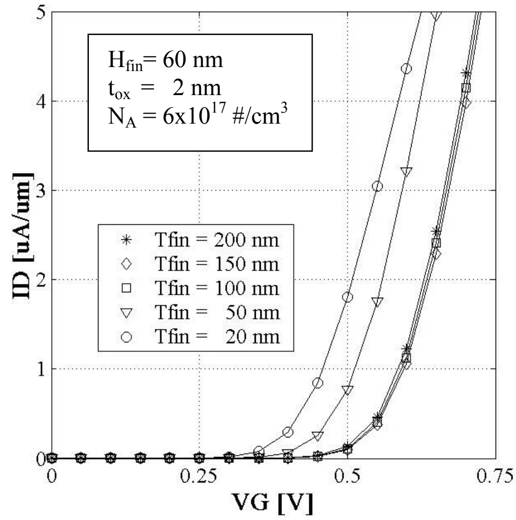

Fig.2 – I_D-V_G characteristics (long-channel FinFET) for different silicon fin thickness (T_{fin}).

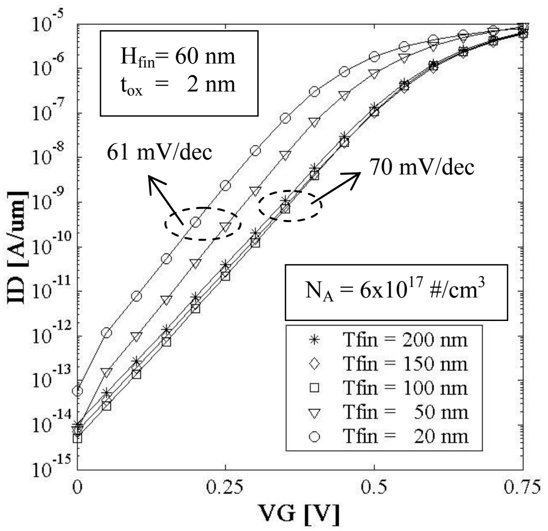

Fig.3 – I_D-V_G characteristics (long channel FinFET - log scale) for different silicon fin thickness (T_{fin}).

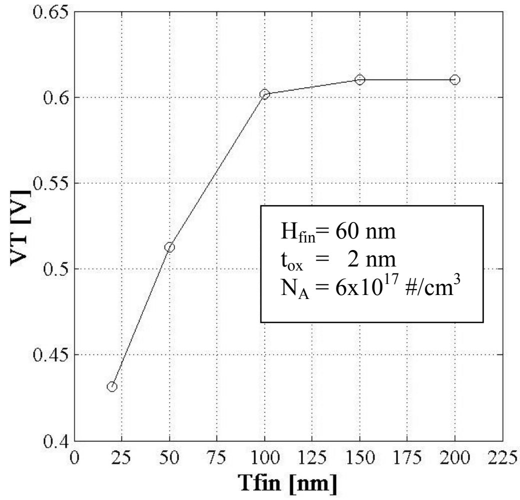

Fig.4 – Threshold voltage (V_T) vs. silicon fin thickness (T_{fin}).

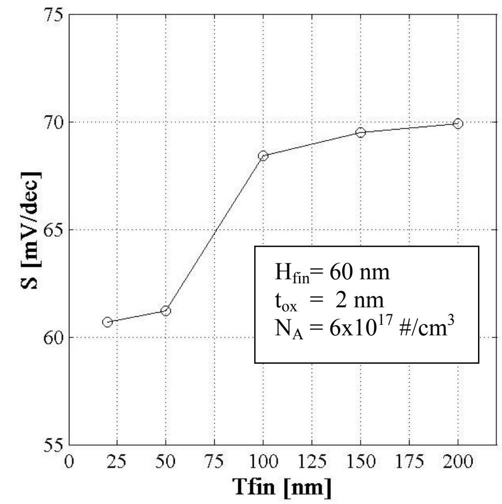

Fig.5 – Sub-threshold slope (S) vs. silicon fin thickness (T_{fin}).

Fig.6 and 7 show the I_D-V_G characteristics (long-channel FinFET) for different N_A and T_{fin} of 20nm and t_{ox} of 2nm. The values of V_T were extracted and are shown in Fig.8 as a function of N_A. The V_T increases as N_A increases for now Q_D contribution to V_T can be compared to the contribution of ϕ_{ms}. This behavior is in accordance with theoretical expressions for FD DG-MOSFETs [1]. The sub-threshold slope (S) is not significantly affected as the fin remains FD (see Fig.7). An analysis of the electrostatic potential has shown that a fin doping around 1x10^{19} #/cm^3 appears to be the limit between a FD and a PD fin. This also agrees with a depletion approximation analysis of a SG-MOS structure where the maximum width of the semiconductor space-charge region (x_{dmax}) is taken at the onset of strong inversion.

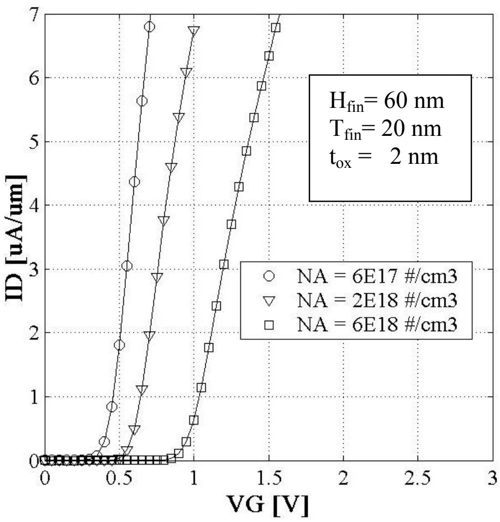

Fig.6 – I_D-V_G characteristics (long-channel FinFET) for different silicon fin doping (N_A).

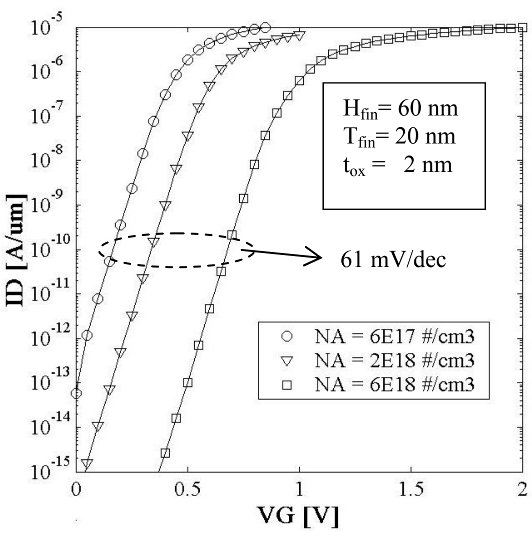

Fig.7 – I_D-V_G characteristics (long channel FinFET - log scale) for different silicon fin doping (N_A).

Tab.1 – Threshold voltage (V_T) and Sub-threshold slope (S) for different values of silicon fin thickness (T_{fin}) and doping (N_A).

V_T (V)	S (mV/dec)	T_{fin} (nm)	t_{ox} (nm)	N_A (#/cm^3)
0.61	70	200	2nm	6E17
0.61	69	150	2nm	6E17
0.60	68	100	2nm	6E17
0.51	61	50	2nm	6E17
0.43	61	20	2nm	6E17
0.59	61	20	2nm	2E18
0.96	61	20	2nm	6E18

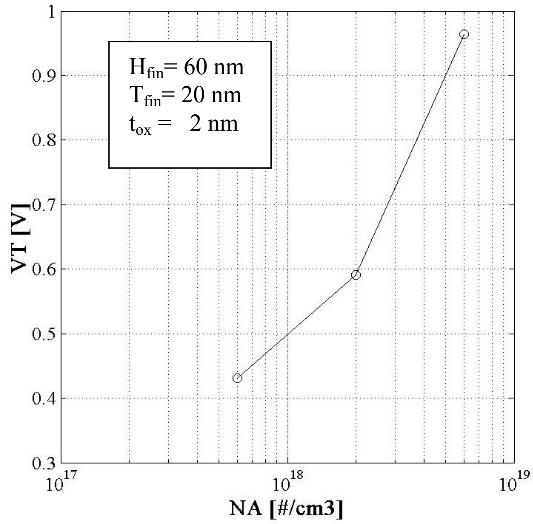

Fig.8 – Threshold voltage (V_T) vs. silicon fin doping (N_A).

4. CONCLUSION

The results of a 3D-numerical simulation of the SOI-FinFET geometry and process parameters for analog circuit design were presented. I_D-V_D characteristics were obtained and the threshold voltage (V_T) and sub-threshold slope (S) dependence with silicon fin thickness (T_{fin}) and doping (N_A) were shown. The influence of a partial depleted (PD) or fully depleted (FD) silicon fin on device characteristics was demonstrated.

5. REFERENCES

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