DESIGN OF LOW-VOLTAGE OPERATIONAL AMPLIFIERS WITH CMOS TECHNOLOGY

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ABSTRACT

In this paper, some topologies used in CMOS operational amplifiers (opamp) are reviewed and two circuits are simulated using the 0.35-µm n-well double-poly CMOS process: the bulk-driven technique uses the substrate of the input differential pair and the adapter technique design a circuit before the differential pair. Both of them are supplied with 1V.

1. INTRODUCTION

Modern VLSI circuits require lower power consumption and the use of lower supply voltages. Generally the modern circuits are mixed-signal circuits where the analog part of the circuitry is operating with the same supply voltage as the digital part. Digital circuitry benefits from technology scaling and reduced supply voltages which result in increased speed and reduced power consumption, respectively.

By the other side, with analog circuits the situation is different because reducing the supply voltage reduces also the dynamic range and speed. Another problem with reduced supply voltage is that many of the conventional analog circuit topologies will not operate anymore due to the fact that as the maximum allowable supply voltage scales down with the minimum feature size, but the threshold voltages V_{TH} of MOS-transistors maintain the same.

As analog circuits require low power supply voltages, the challenges that designers will face in the future at highly scaled technologies and low supply voltages are the limitation of the dynamic range and even circuit functionality; whereas ultra-thin gate oxides are a challenge because they give rise to significant levels of gate leakage current [5]. But, with the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling and the progress of fabrication processes, the integrated circuit market is growing rapidly [6].

The brief study of the topologies will be described in the section 2. The simulated circuits are described in the section 3. In the section 4 the results obtained by simulation are provide; Conclusions are drawn in Section 5 and finally, the references are shown in the section 6.

2. REVIEW OF SOME TOPOLOGIES

One of the main analog building blocks is the operational amplifier. There are four topologies presented here, presented as it follows:

2.1. Parallel-connect complementary differential pairs

In this way, at least one of the two input pairs is active for any input common-mode (CM) level from ground to the supply voltage, VDD. Its circuit is shown at figure 1.

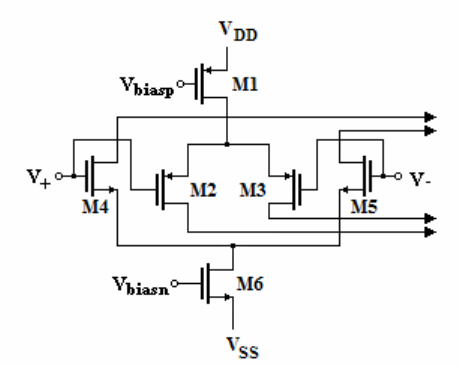

Figure 1 – Complementary differential pair.

However, for extremely low voltages supplies (such as 1V), this topology loses its merit because a dead region in the middle of the input voltage range exists: neither NMOS nor PMOS pairs are turned on in this range.

2.2. Bulk-Driven

As the main limitation for the operation of 1-V circuits arises due to the relatively high value of the threshold voltage with respect to the total supply voltage; a good alternative to increase the input common mode voltage range of a differential pair is to apply the input signal to the bulk terminal (Bulk-Driven) of the input transistors and form the channel in these devices by connecting their gate terminals to an appropriate bias voltage [2-3]. Its circuit is shown in the figure 2.

In this case, the input common mode voltage range of the circuit is extended, as now it is not necessary to spend a part of the input voltage to turn the input devices on.

This circuit will be simulated in the section 3 with a simple two-stage amplifier topology.

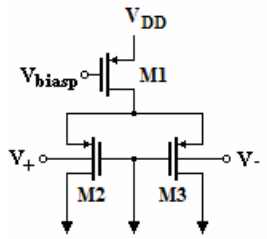

Figure 2 – Bulk-Driven input.

2.3. Adapter circuit

In this topology, a circuit adapter changes the level of voltage in order to bias the gates of the input differential pair. Its block diagram is shown in the figure 3.

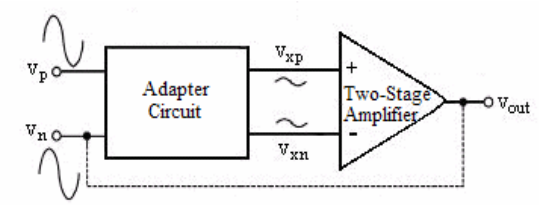

Figure 3 – Adapter circuit.

As the Bulk-Driven technique, this circuit will be simulated in the section 3 with a simple two-stage amplifier topology after the circuit adapter.

2.4. Depletion Transistors

It consists in using of depletion transistor at the input differential pair. This kind of transistor works at different levels of voltage, turning the transistors on with no voltage in its gate. This circuit requires depletion-type MOSFET's, which cannot be fabricated by standard CMOS processes [4], making it not interesting technique. Your symbol is shown in the figure 4.

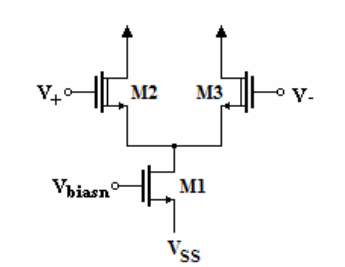

Figure 4 – Depletion-type MOSFET.

3. THE CHOSEN CIRCUITS

In this section, it will be presented the two chosen simulated circuits: Bulk-Driven and Adapter Circuit.

3.1. Adapter circuit

Extracted from [1], the adapter and the ampop circuit are shown in figure 5 and 6, respectively.

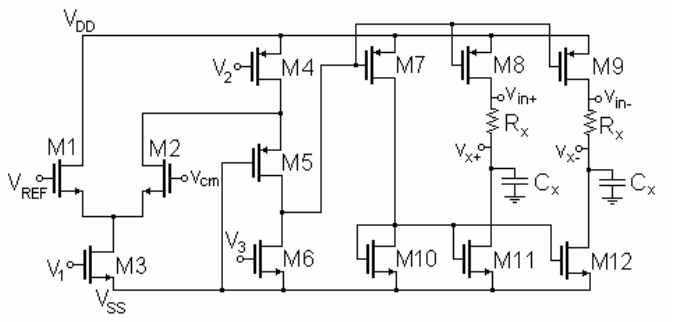

Figure 5 – Adapter circuit.

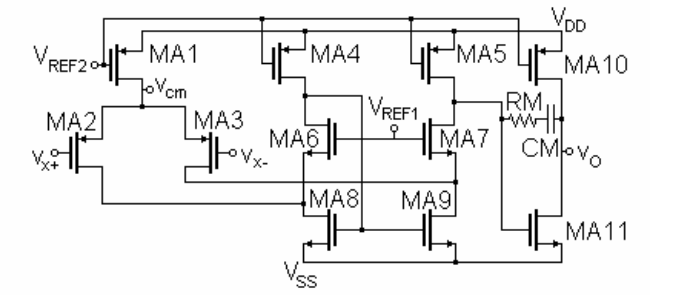

Figure 6 – Two-stage ampop.

The adapter circuit changes the DC level of the input v_{in+} and v_{in-} (about -400mV to PMOS transistors at the differential input pair) in order to bias the input differential pair. It has the two-stage ampop, with a wide swing current mirror as a load in the differential amplifier.

3.2. Bulk-Driven

Extracted from [2], the complete ampop circuit is shown in the figure 7.

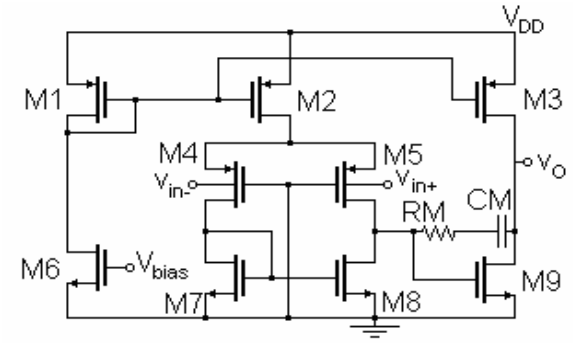

Figure 7 – The Bulk-Driven ampop circuit.

The two-stage amplifier has the bias circuit (M1 and M6), the differential amplifier (M2, M4, M5, M7 and M8) with differential pair modified, the single inverter (M3 and M9) and the compensation circuit (RM and CM).

4. SIMULATION AND RESULTS

In this section, it was presented the simulation and the comparison of the original works of the two chosen circuits. These simulations are of the original work, in order to compare the results.

4.1. Adapter Circuit

Tables 1 and 2 content the geometry of all the transistors of this work and the original work.

Table 1 – Transistors of the adapter circuit.

Device	This Work (µm/µm)	[1] (µm/µm)
M1, M2	12 / 0,6	12 / 0,6
M3	1 / 0,6	-
M4	19 / 0,6	-
M5	130 / 0,6	130 / 0,6
M6	18 / 0,6	-
M7, M8, M9	820 / 0,6	820 / 0,6
M10, M11, M12	270 / 0,6	270 / 0,6
R_x	15kΩ	15kΩ
C_x	0,001pF	-

Table 2 – Transistors of the two-stage amplifier circuit.

Device	This Work (µm/µm)	[1] (µm/µm)
M1, M2	240 / 0,6	240 / 0,6
M3	1000 / 0,6	1000 / 0,6
M4	120 / 0,6	120 / 0,6
M5	40 / 0,6	40 / 0,6
M6	90 / 0,6	90 / 0,6
M7, M8, M9	730 / 0,6	730 / 0,6
M10, M11, M12	260 / 0,6	260 / 0,6
R_x	10kΩ	-
C_x	2pF	-

Some devices are not defined in the original work. There are three current sources in the adapter circuit: based on its current, it was designed the transistors; some capacitors and resistors are not shown too.

The AC analysis was simulated and shown in the figure 8.

Figure 8 shows the DC Gain (an important parameter in the opamp project) and the phase margin, indicates your level of stability. The DC Gain is high (73,3dB) and the phase margin is low (59º). The high value of the DC gain is due the large transistors used in all the circuit (mainly at the two-stage amplifier circuit). The low value of phase margin is due to the number of the extra circuit.

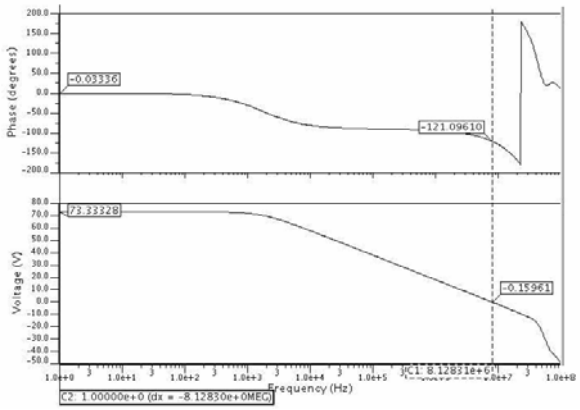

Figure 8 – AC analysis.

Table 3 shows a comparison between the simulated parameters in this work original work.

Table 3 – Simulated parameters of the ampop.

Parameter	This Work	[1]
Biasing Current	160µA	95µA
Bandwidth	8,13MHz	4,13MHz
DC Gain	73,33dB	60dB
Phase margin	59º	83º
Positive Slew Rate	2,5129V/µs	0,86V/µs
Negative Slew Rate	1,5913V/µs	0,8V/µs
Noise density(100kHz)	81,04nV/Hz$^{1/2}$	112nV/Hz$^{1/2}$

Some parameters are better in the original work, like the biasing current and the bandwidth. But in this work, it obtained some better parameters, like the DC Gain and slew rate.

4.2. Bulk-Driven

Tables 4 shows the geometry of all the transistors, in comparison of this work to the original work.

Table 4 – Transistors of the ampop circuit.

Device	This Work	[3]
M1	50 / 5	50 / 5
M2, M3	100 / 5	100 / 5
M4, M5	200 / 20	200 / 20
M6	85 / 10	-
M7, M8	200 / 20	200 / 20
M9	115,2 / 5	100 / 5
RM	140kΩ	140kΩ
CM	1pF	4pF

The transistor M6 is a current source. Its geometry is defined according its current in the original work. The Miller Capacitor is smaller in order to diminish the consumed area.

The AC analysis of Bulk-Driven circuit is shown in the figure 9.

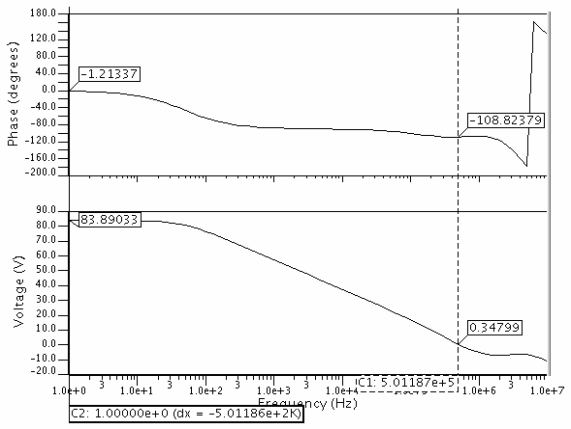

Figure 9 – AC analysis.

The DC Gain and the phase margin, are indicated in the figure 9. The DC Gain is 83,3dB and the phase margin around 72º. The high value of the DC gain is due the large transistors used in all the circuit. This input method has low bandwidth because of the large capacitances of the input differential pair.

Table 5 compares the simulated parameters in this work to the original work.

Table 5 – Simulated parameters of the ampop.

Parameter	This Work	[3]
Biasing Current	6,45µA	5µA
Bandwidth	501kHz	190kHz
DC Gain	83,89dB	83dB
Phase Margin	72º	73º
Positive Slew Rate	0,17V/µs	0,12V/µs
Negative Slew Rate	-0,32V/µs	-0,12V/µs
Noise Density	0,34nV/Hz$^{1/2}$ (10Hz) 0,25nV/Hz$^{1/2}$ (10kHz)	0,46nV/Hz$^{1/2}$ (10Hz) 0,26nV/Hz$^{1/2}$ (10kHz)

The DC Gain and phase margin is very next to the values found at the original work. More current could be necessary in order to have a higher bandwidth than the original work, but still low compared with the adapter circuit.

The input common mode range was simulated in this circuit, shown in the figure 10.

The bulk-driven input improves the DC level (as shown in the figure 10) at the input but larger capacitances (low Bandwidth) appears in the circuit.

5. CONCLUSION

In this work, low-voltage ampop circuits were reviewed and two topologies were simulated. In the adapter circuit, the differences between this work and the original one could be related of the different process used in each one and by the use of different bias circuits in source currents at the adapter circuit from the original work.

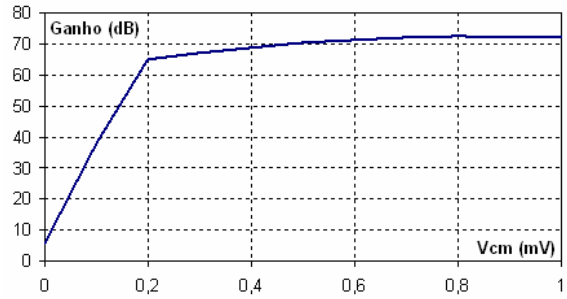

Figure 10 – The Bulk-Driven ampop circuit.

The original work of the bulk-driven technique uses the same process of this work. But the differences between them are from the transistor model: according to [5], its model is not accurate when it is operated in the bulk.

It was possible to see the trade off relationship of the parameters of the opamp: some parameters become better while others become worse.

6. REFERENCES

[1] Baez-Villegas, D. and Silva-Martinez, J., "Quasi Rail-to-Rail very low-voltage OPAMP with a single PMOS Input Differential Pair", IEEE Transactions on circuits and Systems II – Express Briefs, Vol. 53, nº 11, pp. 1175-1179, November 2006.

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[4] Yukizaki, Y., Kobayashi, H., Myono, T., Suzuki, T. and Zhao N., "Low-Voltage Rail-to-Rail CMOS Operational Amplifier Design", Electronics and Communications in Japan, Part 2, Vol. 89, nº 12, 2006. (Translated from Denshi Joho Tsushin Gakkai Ronbunshi, Vol. J89-C, nº 6, June 2006, pp. 402-408).

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