DISTORTION ANALYSIS OF A CMOS BALANCED TRANSCONDUCTOR VALID FOR ALL REGIONS OF OPERATION

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Abstract

The distortion of a balanced transconductor is described. In the analysis, the *Volterra Series* is used to consider the parasitic capacitances influences, and the *Advanced Compact Model (ACM)* MOSFET model is used in order to obtain IIP2 and IIP3 through compact equations. The distortion is examined considering a long channel transistor operating in the whole inversion regime. For simulation, the *Advanced Design System(ADS) of Agilent Technologies* and the BSIM3v3 MOSFET model were used, in absence of a ACM's consistent SPICE model.

1. Introduction

In analog RF circuits, it is necessary a deep knowledge about nonlinearities of circuits, mainly in RF transceivers front-ends. It is particularly important to avoid the intermodulation distortion. Then the understanding of nonlinear behavior of mixers and LNA's have fundamental importance [1]-[3].

The balanced transconductor is a basic component of analog circuits, therefore it's important to understand its nonlinear behavior. Ideally, it has infinite rejection to the second order distortion, consequently it is very used. In presence of offsets and mismatches, the ideal differential transconductor shows second order distortion, that can harm appreciably the circuit operation [4]-[7].

The parasitic capacitance effects become more significant in prediction of intermodulation distortion, in circuits operating with high frequency signals, because they provoke the appearance of even order distortion. Those effects make necessary use of the Volterra Series, because the system becomes a dynamic system or system with memory [3],[7],[8].

This paper analyzes a balanced circuit, considering the parasitic capacitances influences on the circuit's nonlinear behavior. We also offer simple equations valid for all regions of operation. The analysis for short channels is impracticable, because of second order effects like the channel length modulation and the carrier velocity saturation. Those effects make the equations grow considerably, escaping this paper's objective.

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1.1 Transistor Model - ACM

The Advanced Compact Model describes the behavior of MOSFET transistor by compact equations and is very useful for hand analysis. This transistor model is based on the inversion charge density, which uses Unified Control Charge Model (UCCM) as reference model. The UCCM links the terminal voltages of the transistor with inversion charge density. The ACM comprises the whole inversion regime of MOSFET operation at fews equations that have continuous derivatives, an important factor in this analysis [9].

The UCCM version used in this paper is shown in the following:

$$V_P - V_{s(d)} =$$

$$\phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln \left(\sqrt{1 + i_{f(r)}} - 1 \right) \right] \qquad (1)$$

where ϕ_t is the thermal voltage, $i_{f(r)}$ is the forward(reverse) current, normalized for:

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \qquad (2)$$

and V_P is the pinch-off voltage, approximated by [10] as:

$$V_P = \frac{V_g - V_{TH0}}{n} \qquad (3)$$

V_{TH0} is the threshold voltage, n is the slope factor and $V_{s(d)}$ is the source(drain) voltage, respectively. i_f can be called inversion level.

The drain current is given as:

$$I_D = I_f - I_r = (i_f - i_r) \cdot Is \qquad (4)$$

When the transistor is in saturation, we may consider $i_r \ll i_f$, hence:

$$I_D \simeq i_f \cdot I_S \tag{5}$$

1.2 Volterra Series

The *Volterra Series* is a method capable of describing the response of weakly nonlinear systems with memory(Dynamic and nonlinear systems). An important advantage of this method is the ease to use, enabling handy calculation. The basic formula is showed in equation 6.

$$y(t) = \int h_1(\tau_1)x(t-\tau_1)d\tau_1$$

$$+... \int ... \int h_n(\tau_1...\tau_n)x(t-\tau_1)...x(t-\tau_n)d\tau_1...d\tau_n \tag{6}$$

$y(t)$ is the output signal and $x(t)$ is the input signal. Using the nth-order Fourier Transform, it is possible to express the Volterra Series as:

$$y(t) = H_1[x(t)] + H_2[x(t)] + ... + H_n[x(t)] \tag{7}$$

$h_n(\tau_1, \tau_2, ...)$ is called the nth-order Volterra Kernel and $H_n(\omega_1, \omega_2, ...)$ is called the nth-order Volterra Kernel Transform (VKT) [3],[7],[8],[11].

2. Analysis

The examined transconductor is shown in Figure 1. The analysis was made considering that the transistors have long channel, are saturated and both are perfectly matched.

C_{gs1} and C_{gs2} are the Gate-Source capacitances. C_d models the Source-Bulk capacitances of M1 and M2, and the Drain-Bulk capacitance of transistor that implements the current source. Since they are in parallel, they are added.

Evaluating the transconductor in Figure 1, we can find the following expression:

$$i_{d1} + i_{d2} = j \cdot \omega \cdot (C_d + C_{gs1} + C_{gs2}) \cdot v_s \tag{8}$$

Defining $C_t = C_d + C_{gs1} + C_{gs2}$, and using ACM equations, we find i_{f1} by:

$$i_{f1} = i_{d1}/I_s = a \cdot (\frac{v_{rf}}{2} - nv_s) + \frac{b}{2} \cdot (\frac{v_{rf}}{2} - nv_s)^2$$

$$+\frac{c}{6} \cdot (\frac{v_{rf}}{2} - nv_s)^3 \tag{9}$$

and i_{f2} by:

$$i_{f2} = i_{d2}/I_s = a \cdot (\frac{-v_{rf}}{2} - nv_s) + \frac{b}{2} \cdot (\frac{-v_{rf}}{2} - nv_s)^2$$

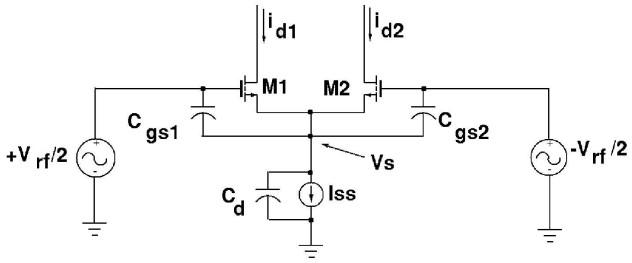

Figure 1: *CMOS balanced transconductor*

$$+\frac{c}{6} \cdot (\frac{-v_{rf}}{2} - nv_s)^3 \tag{10}$$

where:

$$a = \frac{2(\sqrt{1+i_f} - 1)}{n\phi_t} \tag{11}$$

$$b = \frac{2(\sqrt{1+i_f} - 1)}{(n\phi_t)^2\sqrt{1+i_f}} \tag{12}$$

$$c = \frac{2(\sqrt{1+i_f} - 1)}{(n\phi_t\sqrt{1+i_f})^3} \tag{13}$$

Clearly, $a = g_m$, the M1/M2 transconductance.

Using The Volterra Series, we may expand i_{f1} as:

$$i_{d1} = G_1(\omega) \cdot V_{rf} + G_2(\omega_1 + \omega_2) \cdot V_{rf}^2 +$$

$$G_3(\omega_1 + \omega_2 + \omega_3) \cdot V_{rf}^3 \tag{14}$$

where G_1, G_2 and G_3 are the first order, second order and third order VKT.

The IIP2 and the IIP3 were used to measure the distortion. We can define them as:

$$IIP2 = \left|\frac{G_1}{G_2}\right| \tag{15}$$

$$IIP3 = \left|\sqrt{\frac{4G_1}{3G_3}}\right| \tag{16}$$

Replacing the VKT, we found the following results:

$$IIP2 = 4 \cdot k \cdot n \cdot \phi_t \cdot \left|\frac{\frac{n \cdot g_m}{C_t} + j\omega}{j\omega}\right| \tag{17}$$

$$IIP3 = \beta \cdot \left|\frac{\frac{n \cdot g_m}{C_t} + j\omega}{\left(\frac{3k-1}{2k-1}\right)\frac{n \cdot g_m}{C_t} + j\omega}\right|^{1/2} \tag{18}$$

where $k = \sqrt{1+i_f}$ and $\beta = \frac{4\sqrt{2} \cdot n \cdot \phi_t \cdot k^{3/2}}{\sqrt{2k-1}}$.

3. Results

The ADS Agilent was used as simulation program. The technology AMIS $0.35\mu m$ and transistors with $W/L = \frac{20\mu m}{4\mu m}$ were used. The variation in parasitic capacitances with the inversion regime of operation was disregarded, therefore they were considered constants, influencing little in results.

In figure 2, the *IIP2 vs.* i_f was ploted for three frequencies: 1 kHz, 100 kHz e 5 MHz.

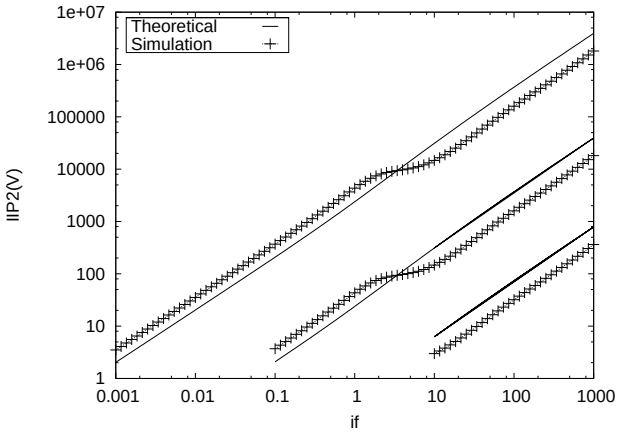

Figure 2: *Prediction and Simulation of IIP2 for 1 kHz, 100 kHz and 5 MHz*

The discontinuity observed in moderate inversion may be explained by the mathematical interpolation made in this region by BSIM 3V3 model.

In figure 3, *IIP2 vs. frequency* was ploted for $i_f = 500$.

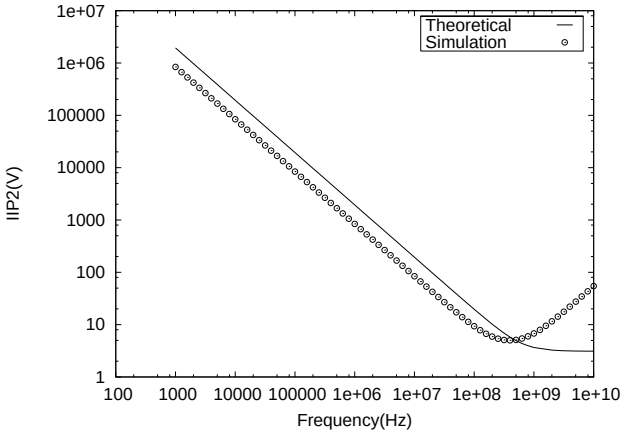

Figure 3: *IIP2 vs. Frequency*

Clearly, the frequency has huge influence at the IIP2, proving the effect of parasitic capacitances about the distortion. The difference on high frequencies are due to the disregarded effects, possibly a zero caused by others capacitances, such as Gate-Drain Capacitance.

In figure 4, the *IIP3 vs.* i_f was ploted for 100 kHz:

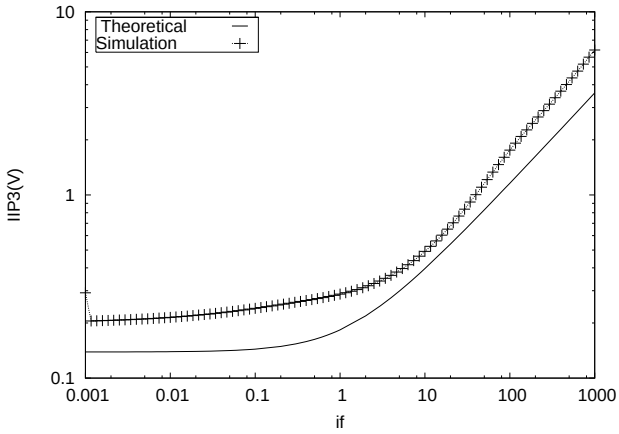

Figure 4: *Prediction and Simulation of IIP3 vs.* i_f *for 100 kHz*

Both curves have the same behavior, however there is a little difference in moderate inversion, explained previously. The IIP3 is almost constant in weak inversion, rising considerably in the beginning of moderate inversion.

Analyzing (18), it is easy to note that the IIP3 is almost constant, only varying for very high frequencies and high inversion level, therefore that effect may be disregarded.

4. Conclusion

Using the Volterra Series, we obtained simple equations to predict the distortion of a balanced transconductor, being an important tool for hand design. The use of Volterra Series was important to analyze the memory effect of parasitic capacitances and to obtain compact equations. ACM MOSFET model was important to describe the distortion for all regions of operation, using few parameters and simple analytical equations. The parasitic capacitances and the frequency have a wide influence at second-order distortion, making C_t an important design parameter. The IIP3 doesn't intensely vary with frequency, but it is very low in weak inversion, being a challenge for designer focused in distortion.

5. Acknowledgements

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